

Taos Schematics Skylake/Kabylake-U

2016-12-23

REV : A00

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DY : None Installed

UMA: UMA only installed

OPS: DISCRTE OPTIMUS installed

2.DIS



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Title

Cover Page

Size
A3

Document Number

Taos KBL-U

Rev

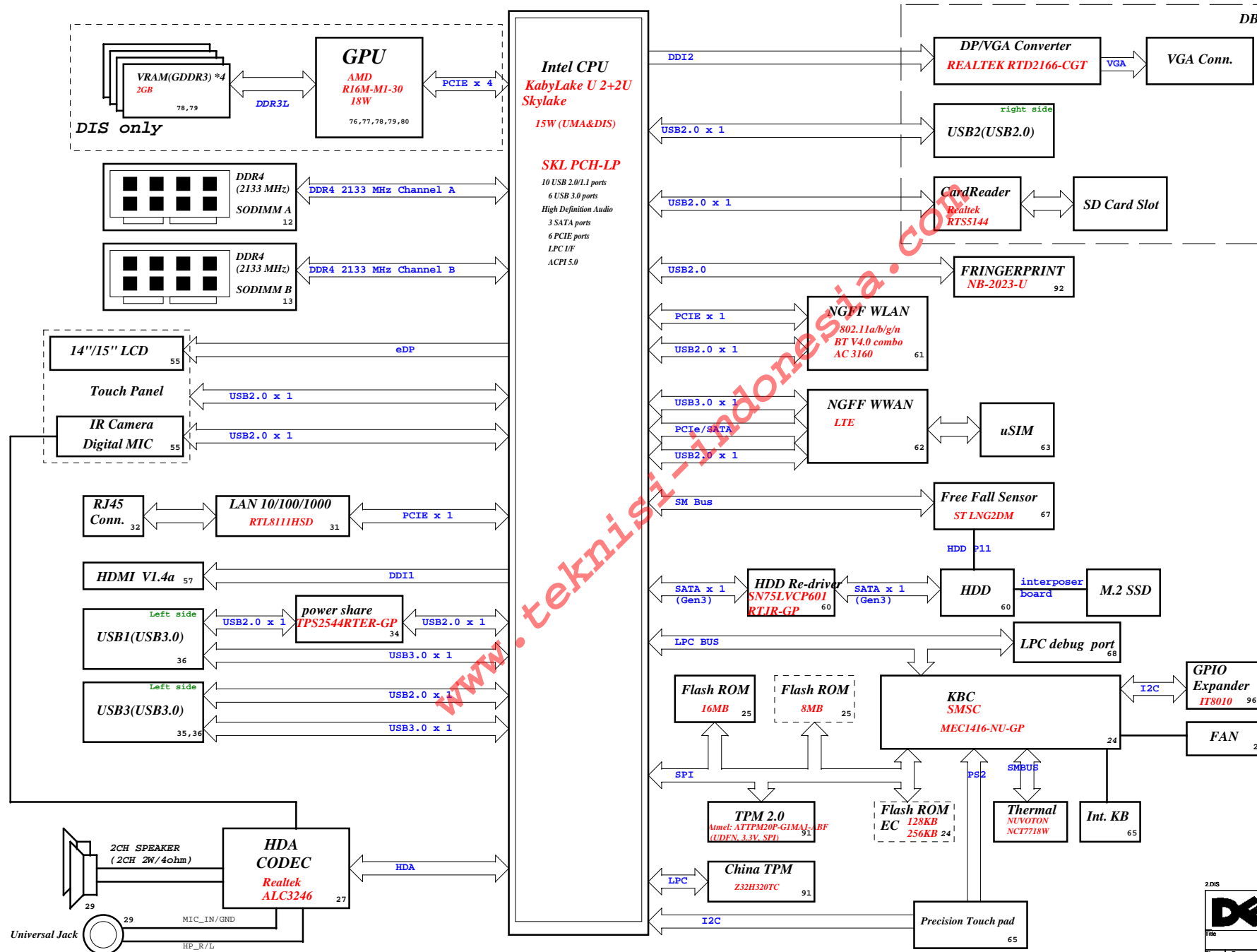
X00

Date: Monday, December 26, 2016

Sheet 1 of 105

Project code:
Taos14 -->4PD09Z010001
Taos15 -->4PD0A1010001
PCB P/N: 16852
Revision: A00

Taos KBL-U/SKL-U Block Diagram




CHARGER		44
BQ24786RUYR-GP		
INPUTS	OUTPUTS	
AD+	DCBATOUT	
SYSTEM DC/DC		45
SY8288CRAC-GP		
INPUTS	OUTPUTS	
	PWR 5V	
DCBATOUT	5V_S5	
	5V_AUX_S5	
CPU Core Power		46-50
NCP81208MNTXG		
NCP81382MNTXG*2		
NCP81253MNTBG		
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE	
DCBATOUT	+VCCGT	
DCBATOUT	+VCCSA	
DDR4		51
APW8861QBI-TRG-GP		
INPUTS	OUTPUTS	
DCBATOUT	1D2V_S3	
	0D6V_S0	
CPU DCDC-V1D00A		53
AOZ2261QI-10-GP-U		
INPUTS	OUTPUTS	
DCBATOUT	1D0V_S5	
LDO-V1D8V		54
APL5930KAI-TRG-GP		
INPUTS	OUTPUTS	
3D3V_S5	1D8V_S5	
CPU VCCPRIM_CORE		11
INPUTS	OUTPUTS	
1D0V_S5	+VCCPRIM_CORE	
5V/3V_S0		40
G5016KDLU		
INPUTS	OUTPUTS	
5V_S5	5V_S0	
3D3V_S5	3D3V_S0	
VCCSTG		40
APE8939GN3-GP		
INPUTS	OUTPUTS	
5V_S5	+VCCIO	
	+VCCSTG	
VCCST		40
APE8939GN3-GP		
INPUTS	OUTPUTS	
5V_S5	+V1_000_CPU	
	+VCCSTG_CPU	
PCB LAYER		
L1:Top		
L2:VCC		
L3:Signal		
L4:Signal		
L5:GND		
L6:Bottom		

Main Func = CPU

(Blanking)

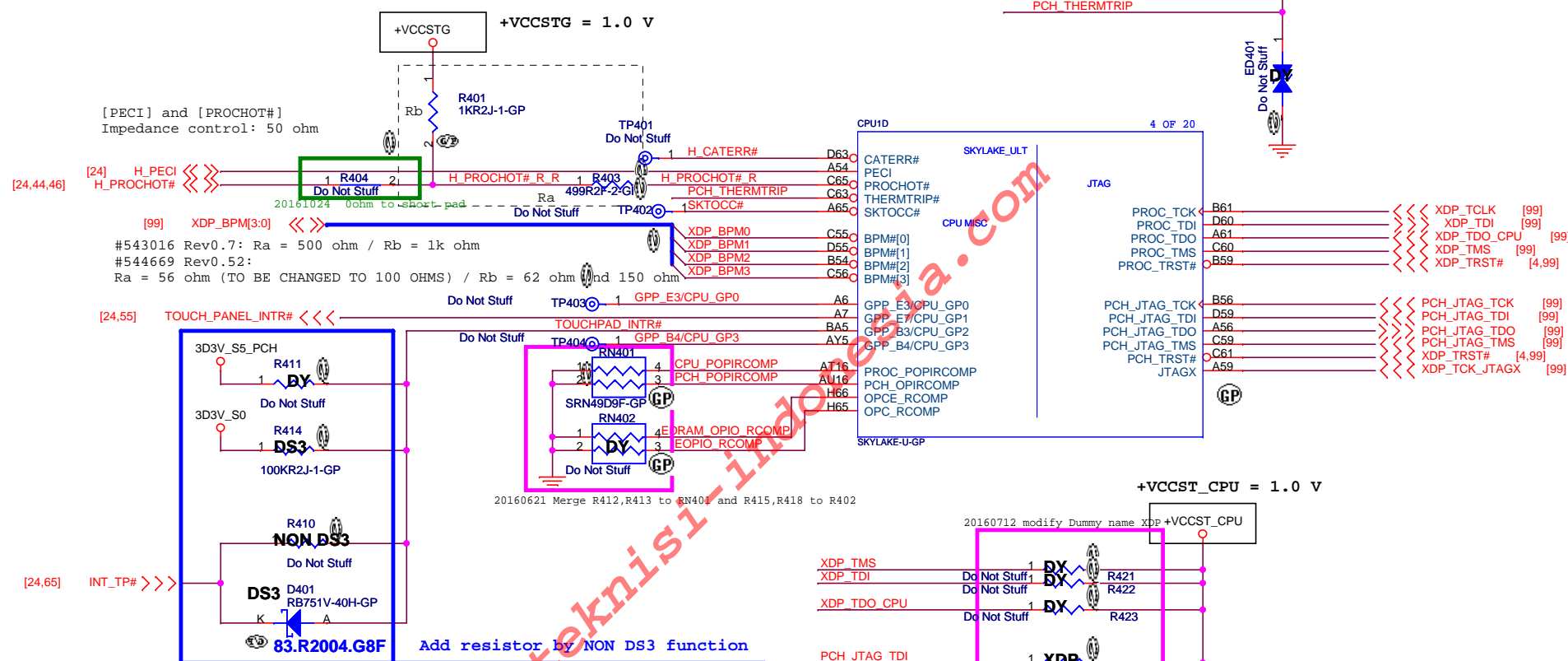
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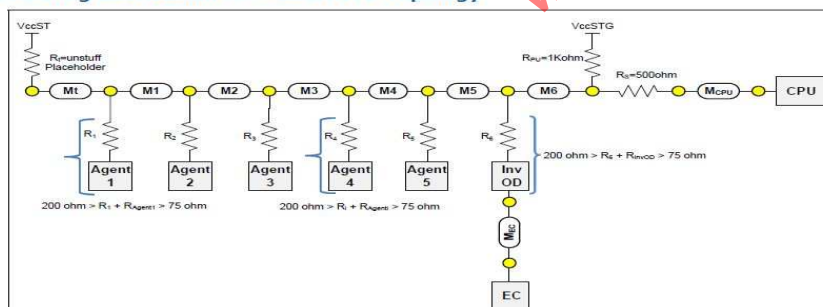
Main Func = CPU

#544669 CRB Rev0.52

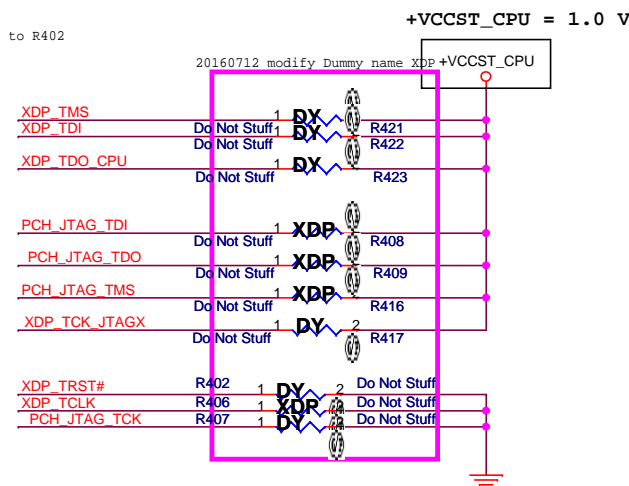


(#543016) PROCHOT# Routing Guidelines

Figure 10-1. Routing Illustration for PROCHOT# Topology



Main route (M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches



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Title	CPU_ (JTAG/CPU SIDE BAND)
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Size	Document Number
Custom	

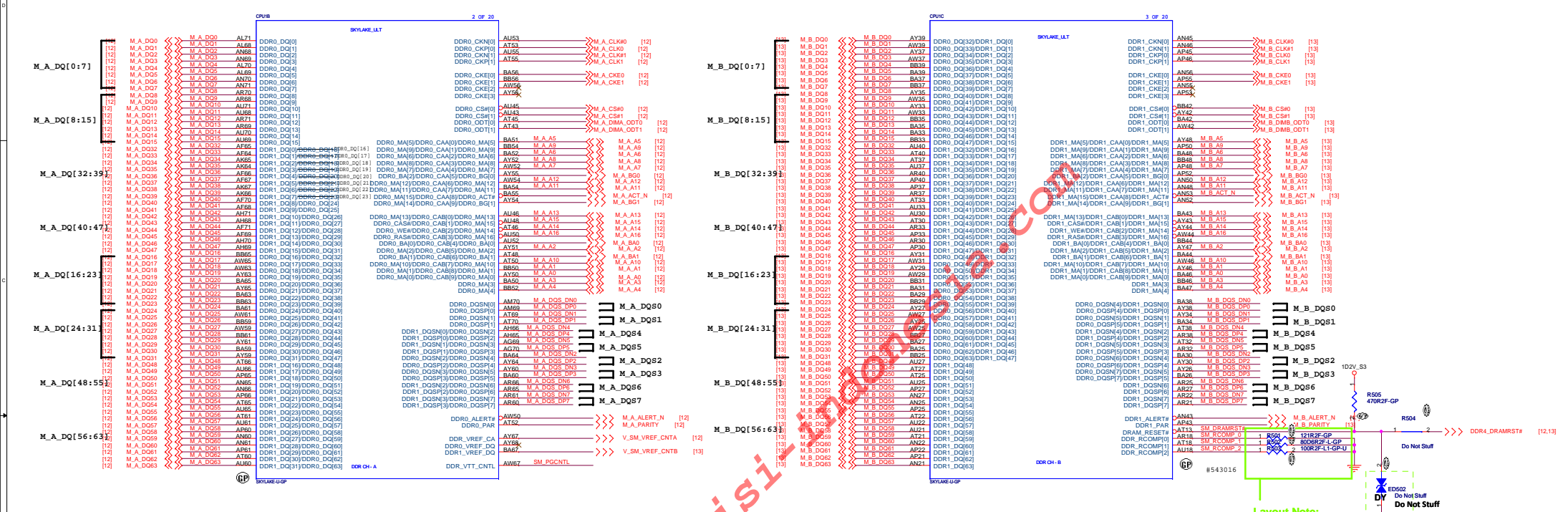
Taos KBL-U

Rev	X00
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Date: Monday, December 26, 2016

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DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel.
Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to CLK# and Strobe within a channel is not allowed.

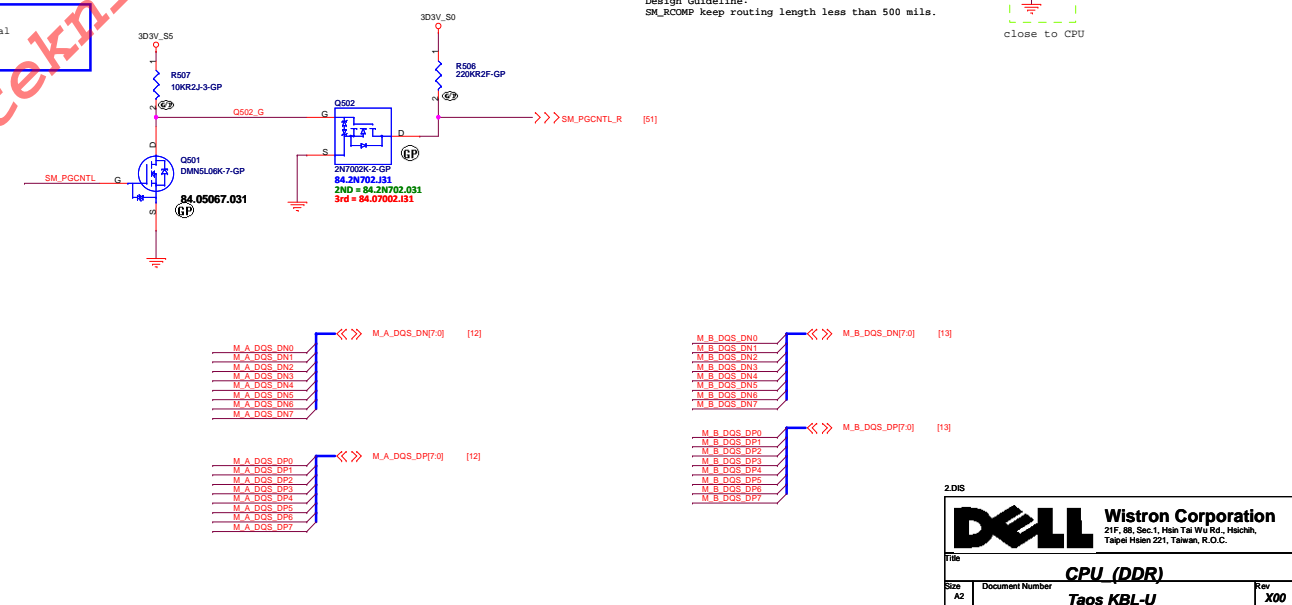
PDG: DDR/ODT

4.17 SKL U and SKL Y System Memory ODT Signal Connectivity Details

Processor	Memory Type	Side	Signal	Rule	Notes
SKL-Y	LPDDR3 Memory Down	Processor	DDR0_ODT[0]	Processor's ODT[0] connected to DRAM's ODT. T-topology connection	1,2
		DRAMs	DDR0_ODT[0]	Processor's ODT[0] connected to DRAM's ODT. T-topology connection	1,2
SKL-U	LPDDR3 Memory Down	Processor	DDR0_ODT[1:0]	Processor's ODT[0] connected to DRAM's ODT. T-topology connection.	1,2
		DRAMs	DDR0_ODT[1:0]	Processor's ODT[1] not connected.	1,2
DDR3L Memory Down	Processor	Processor	DDR0_ODT[1:0]	Processor's ODT[0] connected to DRAM's Rank0 ODT.	3,4
		DRAMs	DDR0_ODT[1:0]	Processor's ODT[1] not used, Processor's Rank1 ODT connected.	3,4
DDR3L SO-DIMM	Processor	Processor	DDR0_ODT[1:0]	Processor's ODT[1:0] connected to DIMM's Rank0 ODT.	1,3
		DIMMs	DDR0_ODT[1:0]	Processor's ODT[1] not connected.	1,3
DDR3L Mixed Memory Down	Processor	Processor	DDR0_ODT[1:0]	DDR0_ODT[1:0] connected to DIMM's Rank0 ODT. Processor's Rank0 ODT connected to DIMM's Rank0 ODT.	3,4
		DRAMs	DDR0_ODT[1:0]	Processor's ODT[1] not connected to DIMM's Rank1 ODT. Processor's Rank1 ODT connected to DIMM's Rank1 ODT. Processor's Rank2 ODT connected to DIMM's Rank2 ODT. Processor's Rank3 ODT connected to DIMM's Rank3 ODT.	3,4
DDR4 Memory Down	Processor	Processor	DDR0_ODT[1:0]	Processor's ODT[0] connected to DRAM's Rank0 ODT. Processor's ODT[1] connected to DRAM's Rank1 ODT.	1,2
		DRAMs	DDR0_ODT[1:0]	Processor's ODT[1] not connected.	1,2
DDR4 SO-DIMM	Processor	Processor	DDR0_ODT[1:0]	Processor's ODT[0] connected to DIMM's Rank0 ODT. Processor's ODT[1] connected to DIMM's Rank1 ODT.	1,2
		DIMMs	DDR0_ODT[1:0]	Processor's ODT[1] not connected.	1,2

Notes:

- For additional ODT signal connection details, reference the Customer Reference Board (CRB) schematics and board files (BUP2 - SKL-U (DDR3L), BUP3 - SKL-U (DDR3L), BUP4 - SKL-U (DDR3L)).
- Processor's Rank0 ODT is high impedance (HIZ) when the processor is in power-down state. Processor's Rank1 ODT is high impedance (HIZ) when the processor is in power-down state. Processor's Rank2 ODT is high impedance (HIZ) when the processor is in power-down state. Processor's Rank3 ODT is high impedance (HIZ) when the processor is in power-down state.
- DDR3L ODT input is high impedance (HIZ). HIZ NCH is defined by R105 in both ranks, when a Rank receives write command R# valid (set by R105 after power transition). Otherwise ODT is high impedance (HIZ) NCH (high-Z).
- These guidelines are related to DDR3L, supported Memory down topologies only. 2R x16 DCP single side, 2R x16 DCP dual side and 2R x16 DCP dual side.

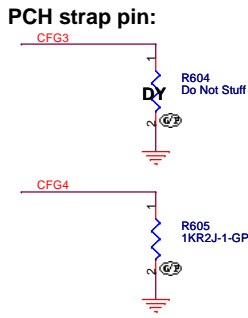
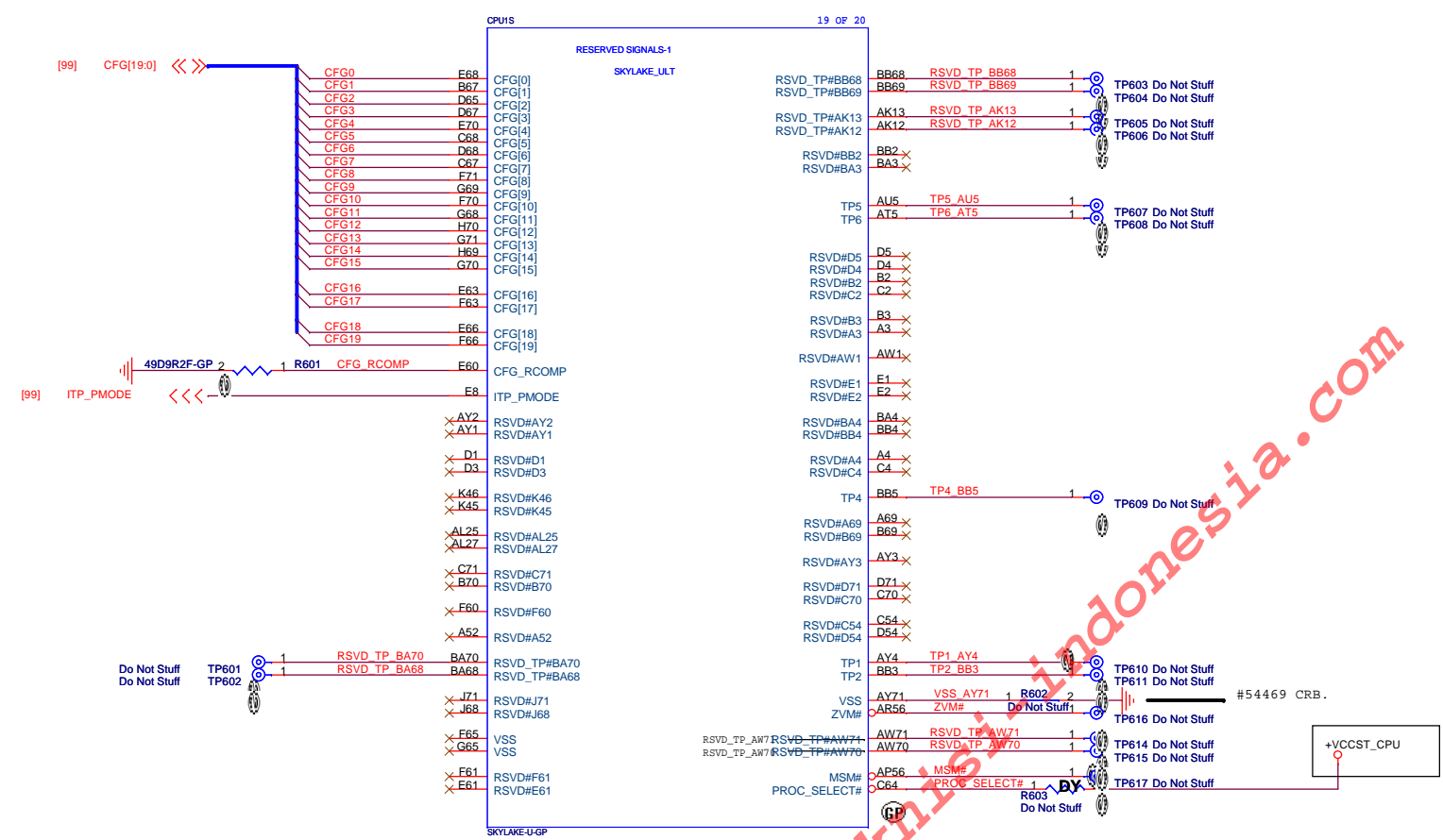


Layout Note:

Design Guideline:
SM_PGNTL keep routing length less than 500 mils.



Main Func = CPU



[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
	1 : DISABLED

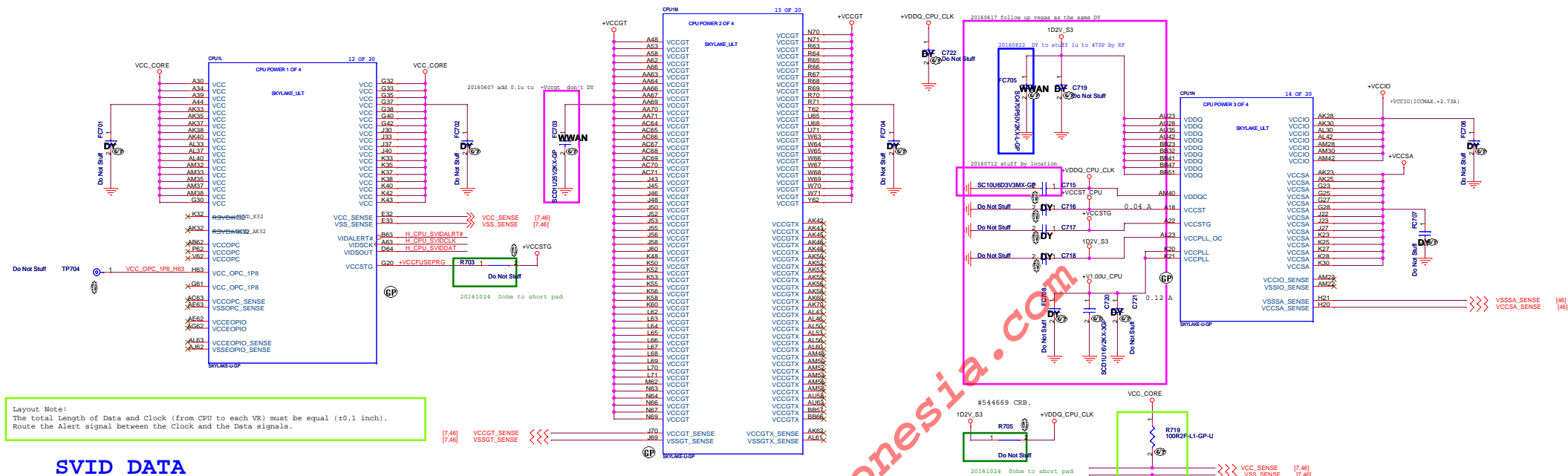
DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port.
	1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

CFG TERMINATIONS

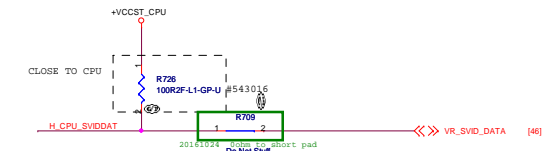
20140807 david

#544669 Rev0.52 (CRB)

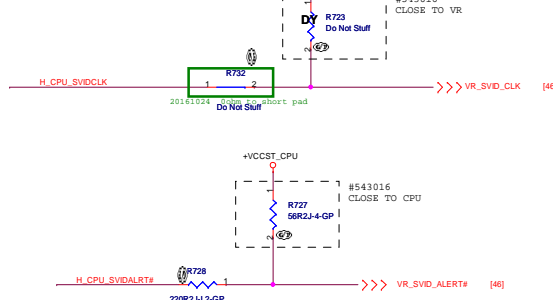
SKL(#543016):
Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*



SVID DATA



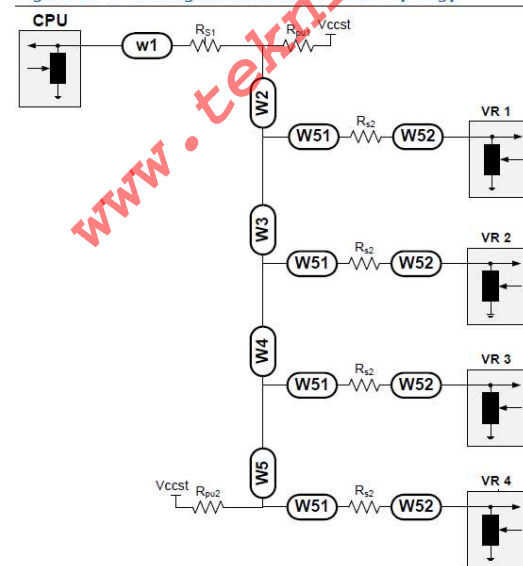
SVID CLOCK



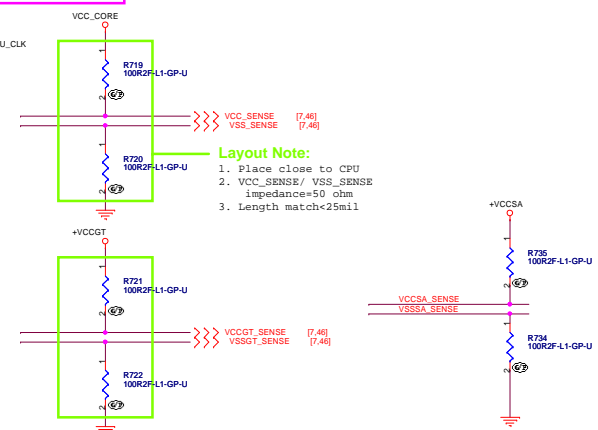
SVID_543016:

Table 10-10.SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W6 [inches]	W52 [inches]	R ₅₀₁ [Ω]	R ₅₀₂ [Ω]	R ₅₁ [Ω]	R ₅₂ [Ω]	V _{CC} [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	



- Layout Note:
 1. Place close to CPU
 2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
 3. Length match<25mil




Main Func = CPU

(Blanking)

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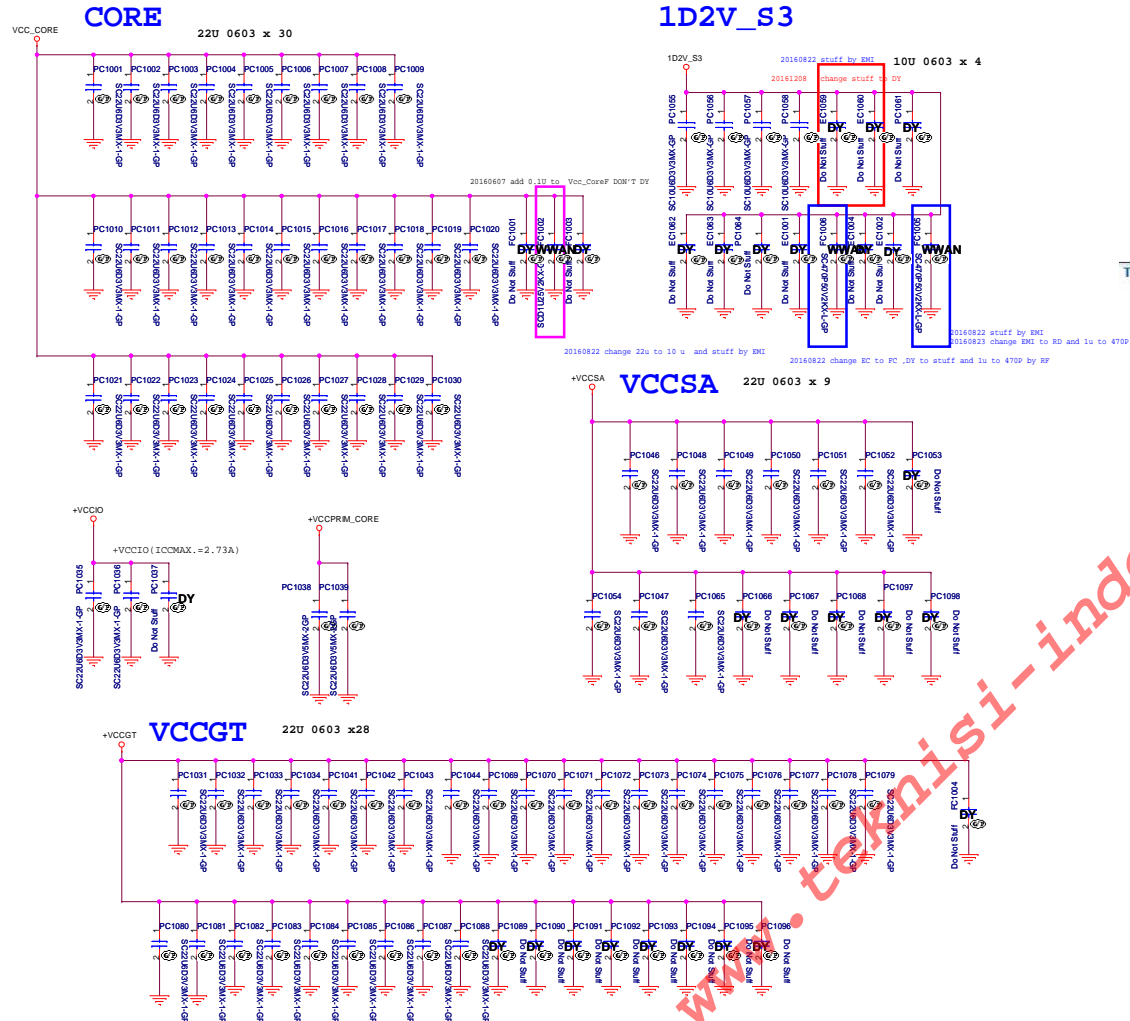


Table 53-3. SKL U Bulk Decoupling Requirements

Bulk Decoupling Locations	Requirements	Notes
VCC Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
VCCGT Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at backside side near to VR output
VCCGTx Power Plane at VR output	2x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
VCCIO Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
VCCSA Power Plane at VR output	2x 47uF 0805	Additional components needed when supporting 23e

Note: These requirements are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 1 of 2)

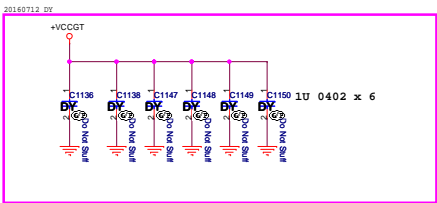
Domain	Backside cap	Primary side cap	Placement guideline
VCC	9x 22uF 0603		Place on secondary side, underneath the package
	7x 10uF 0402		
	15x 1uF 0201		
		8x 47uF 0805 (6.3V)	Place as close to the package as possible
VCCGT	10x 10uF 0402		Place on secondary side, underneath the package
	12x 1uF 0201		
		3x 47uF 0805 (6.3V)	Place as close to the package as possible
		7x 22uF 0603	Place as close to the package as possible
		3x 47uF 0805	Additional components needed when supporting 23e
VCCGTx	8x 10uF 0402		Place on secondary side, underneath the package
		8x 22uF 0603	Only needed when supporting 23e
VCCSA	7x 10uF 0402		Place on secondary side, underneath the package
	7x 1uF 0201		
		6x 10uF 0402	Place as close to the package as possible
VCCIO	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
VDDQ	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 10uF 0402	Place as close to the package as possible
VDDQC	1x 1uF 0201		Place on secondary side, underneath the package
VCCPLL	1x 1uF 0402		Place as close to the package as possible
VCCST	1x 1uF 0402		Place as close to the package as possible

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

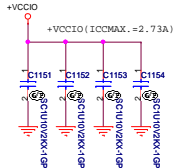
Domain	Backside cap	Primary side cap	Placement guideline
VCCSTG	1x 1uF 0402		Place on secondary side, underneath the package
VCCEOPTIO	2x 10uF 0402		Place on secondary side, underneath the package
VCCOPC	1x 10uF 0402		Place on secondary side, underneath the package
	6x 1uF 0201		

2.0S

Main Func = CPU



VCCIO



PCH DERIVED RAILS

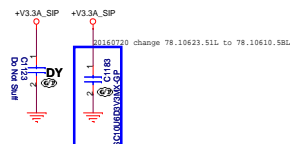
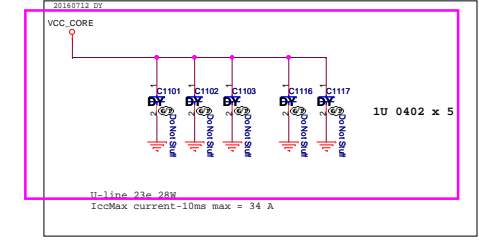
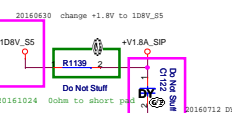
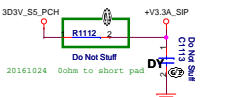
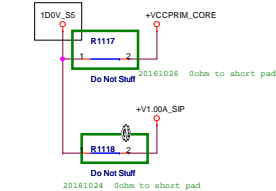


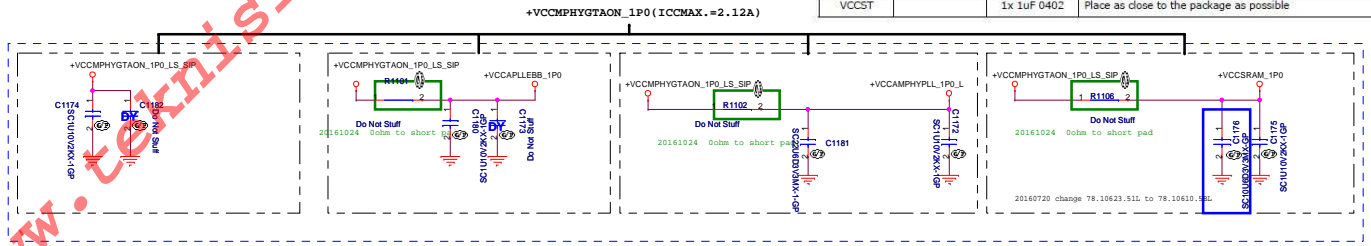
Table 53-3. SKL U Bulk Decoupling Requirements

Bulk Decoupling Locations	Requirements	Notes
VCC Power Plane at VR output	1x 220uF (@4.5mΩ ESR) 1x 220uF (@4.5mΩ ESR)	Placed at primary side near to VR output Placed at backside near to VR output
VCCGT Power Plane at VR output	2x 220uF (@4.5mΩ ESR) 1x 220uF (@4.5mΩ ESR)	Placed at primary side near to VR output Additional components needed when supporting 23e
VCCGTx Power Plane at VR output	1x 220uF (@4.5mΩ ESR)	Placed at primary side near to VR output Only needed when supporting 23e
VCCIO Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output
VCCSA Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output

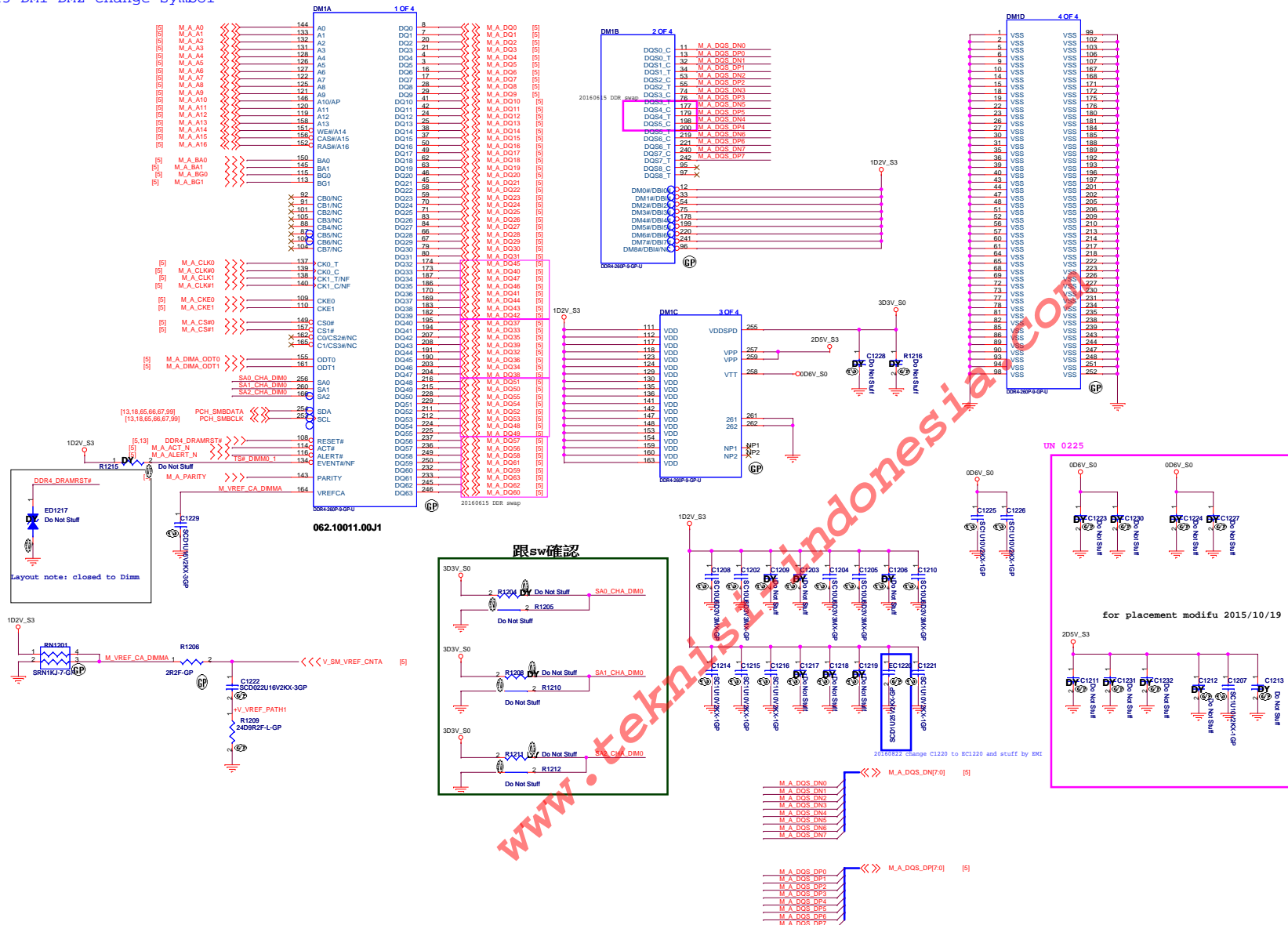
Note: These requirements are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 1 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCC	9x 22uF 0603 7x 10uF 0402 15x 1uF 0201		Place on secondary side, underneath the package
VCCGT	10x 10uF 0402 12x 1uF 0201	8x 47uF 0905 (6.3V) ¹ 8x 10uF 0402	Place as close to the package as possible
VCCGTx	8x 10uF 0402	3x 47uF 0905 (6.3V) ¹ 7x 22uF 0603 3x 47uF 0805 5x 22uF 0603	Place as close to the package as possible Additional components needed when supporting 23e
VCCSA	7x 10uF 0402 7x 1uF 0201	6x 10uF 0402	Place as close to the package as possible
VCCIO	2x 10uF 0402 4x 1uF 0201	4x 1uF 0402	Place as close to the package as possible
VDDQ	2x 10uF 0402 4x 1uF 0201	4x 10uF 0402	Place as close to the package as possible
VDDQC	1x 1uF 0201		Place on secondary side, underneath the package
VCCPLL	1x 1uF 0402		Place as close to the package as possible
VCCST	1x 1uF 0402		Place as close to the package as possible



20160815 DM1 DM2 change symbol




2.DIS

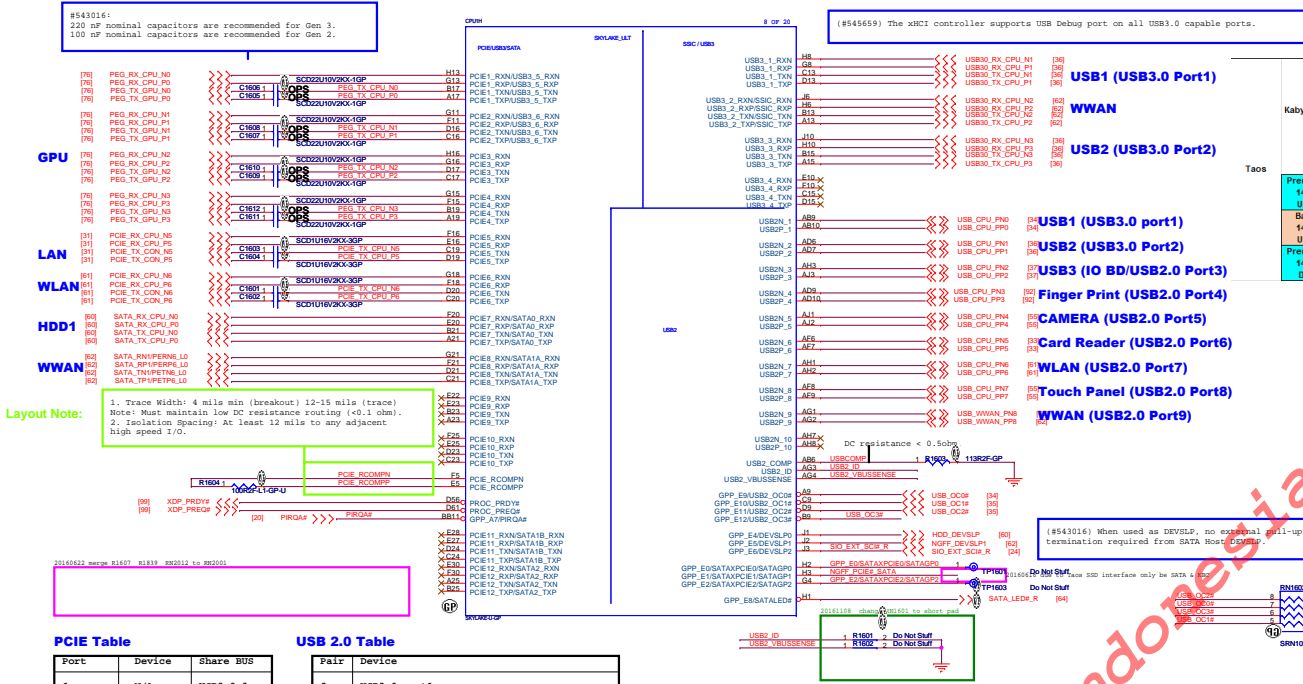
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Size A4	Document Number Taos KBL-U		Rev X00
Date: Monday, December 26, 2016		Sheet 14	of 105

Main Func = PCH



update 0509																				
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16			
Lake U	USB3-1 OTG	USB3-2	USB3-3	USB3-4	PCle-1		PCle-2		PCle-3		PCle-4		PCle-5		PCle-6					
					USB8-5		USB8-6		GRE		GRE		GRE		PCle-6		PCle-7		PCle-8	
															SATA 5		SATA1		PCle-9	
																	GRE		PCle-10	
																	SATA 11		PCle-11	
														SATA 2		PCle-12				
						X2		X2		X2		X2		X2		X2				
						X4		X2		X4		X2		X4		X2				
						PCle Controller #1		PCle Controller #2 (Cycle Router 2)		PCle Controller #3 (Cycle Router 3)										
								LOM		M.2 3030 (WLAN)		HDD SATA only 20pin Conn		M.2 3042 (SSD Cache)						
										LOM		M.2 3030 (WLAN)		HDD SATA only 20pin Conn		M.2 3042 (SSD Cache)				
										LOM		M.2 3030 (WLAN)		HDD SATA only 20pin Conn		M.2 3042 (SSD Cache)				
										LOM		M.2 3030 (WLAN)		HDD SATA only 20pin Conn		M.2 3042 (SSD Cache)				

USB 2.0 (10 ports)															
USB2-1 OTG	USB2-2	USB2-3	USB2-4	USB2-5	USB2-6	USB2-7	USB2-8	USB2-9	USB2-10						
Ext Port 1	Ext Port 2	Ext Port 3 2.0 only	FPR	UF Camera	SD Reader	M.2 3030 (BT)	LCD Touch	M.2 3042 (WWAN)		LCD	VGA	HDMI			
Ext Port 1	Ext Port 2	Ext Port 3 2.0 only	FPR	UF Camera	SD Reader	M.2 3030 (BT)	LCD Touch	M.2 3042 (WWAN)		LCD	VGA	HDMI			
Ext Port 1	Ext Port 2	Ext Port 3 2.0 only	FPR	UF Camera	SD Reader	M.2 3030 (BT)	LCD Touch	M.2 3042 (WWAN)		LCD	VGA	HDMI			

PCIe Table		
Port	Device	Share BUS
1	N/A	USB3_0_3
2	N/A	USB3_0_4
3	WLAN	
4	LAN	
5 (L0-L3)	GPU	
6 (L3)	HDD	SATA0
6 (L2)	N/A	
6 (L0-L1)	N/A	

USB 2.0 Table		
Pair	Device	
0	USB3.0 port1	
1	USB3.0 Port2	
2	USB2.0 Port3 (IOBD)	
3	Finger print	
4	CAMERA	
5	Card Reader	
6	Touch Panel	
7	WLAN	

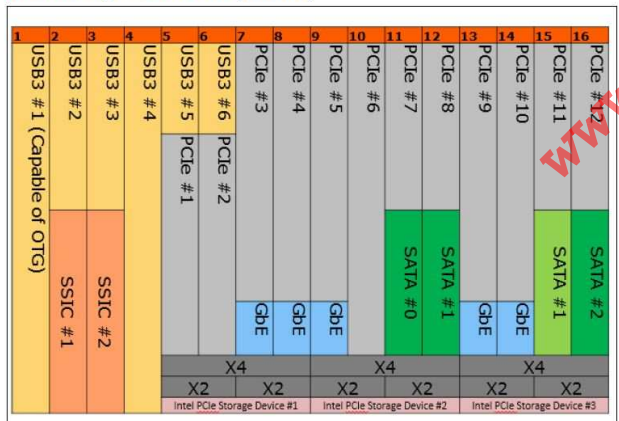
Table 24-2. PCI Express* Port Feature Details

SKL	Max Device (Ports)	Max Lanes	PCIe* Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s)		
						x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

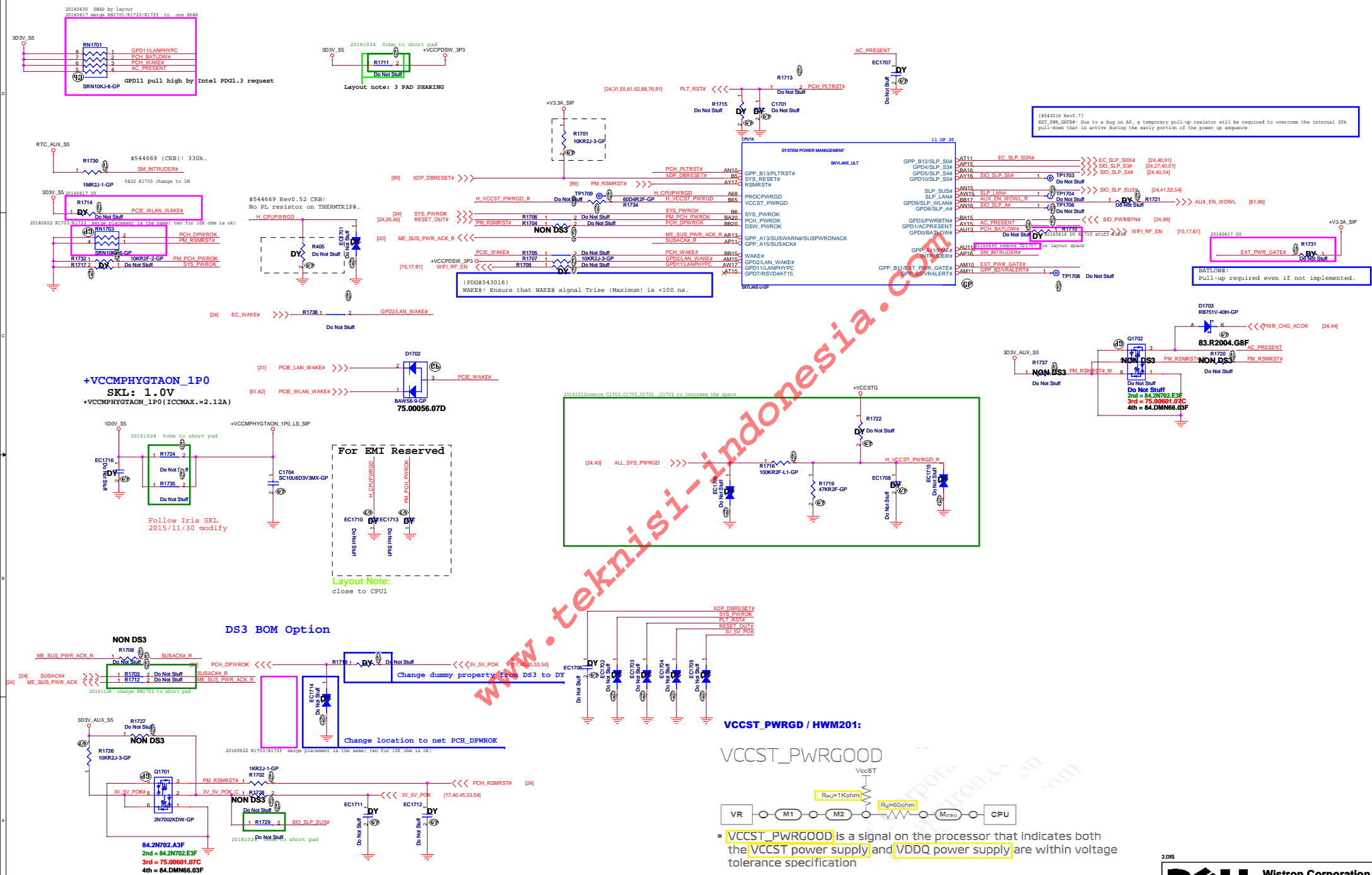
Table 24-3. PCI Express* Link Configurations Supported

SKL	PCIe Link Config	PCI Express* Lanes											
		1	2	3	4	5	6	7	8	9	10	11	12
U	1x4	Port1				Port5				Port9			
	2x2	Port1		Port3		Port5		Port7		Port9		Port11	
	1x2 + 2x1	Port1	Port3	Port4	Port5	Port7	Port8	Port9	Port10	Port11	Port12		
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12
Y	1x4	Port1				Port5							
	2x2	Port1		Port3		Port5		Port7					
	1x2 + 2x1	Port1	Port3	Port4	Port5	Port7	Port8						
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8				
	1x2									Port9			
	2x1									Port9	Port10		

Figure 3-1. HSI0 Muxing on SKL PCH-LP (U Series)



5
Main Func = PCH



```
#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST
```


Main Func = PCH

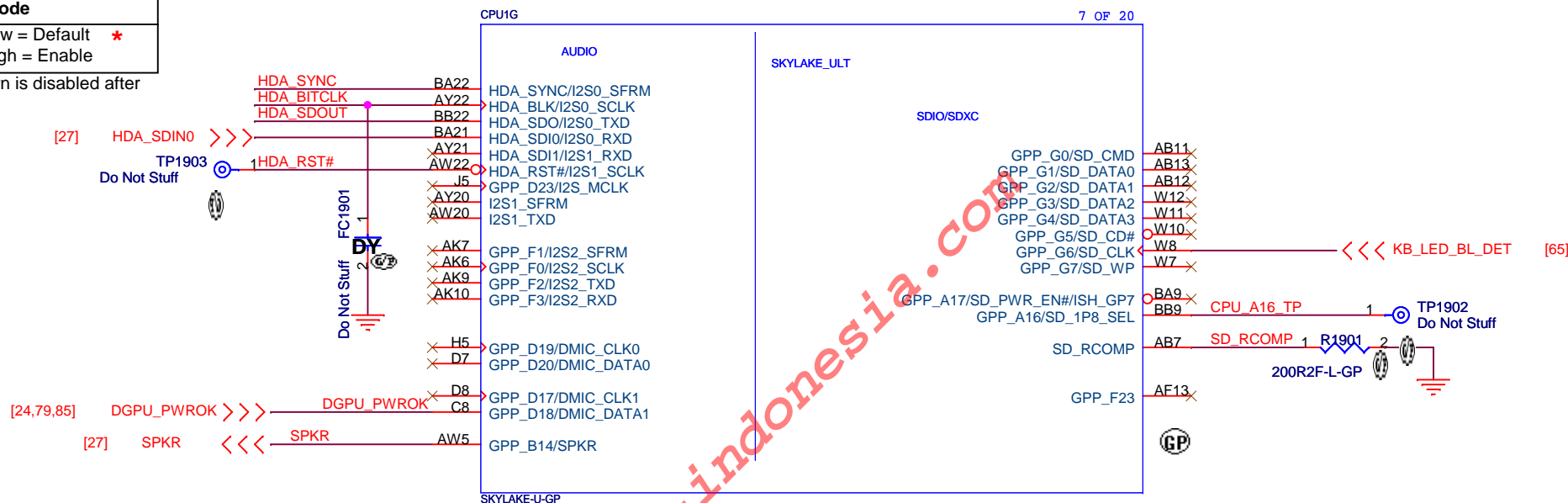
PCH strap pin:

Flash Descriptor Security Override/ Intel ME Debug Mode

HDA_SDOUT

Low = Default *
High = Enable

The internal pull-down is disabled after
PLTRST# deasserts



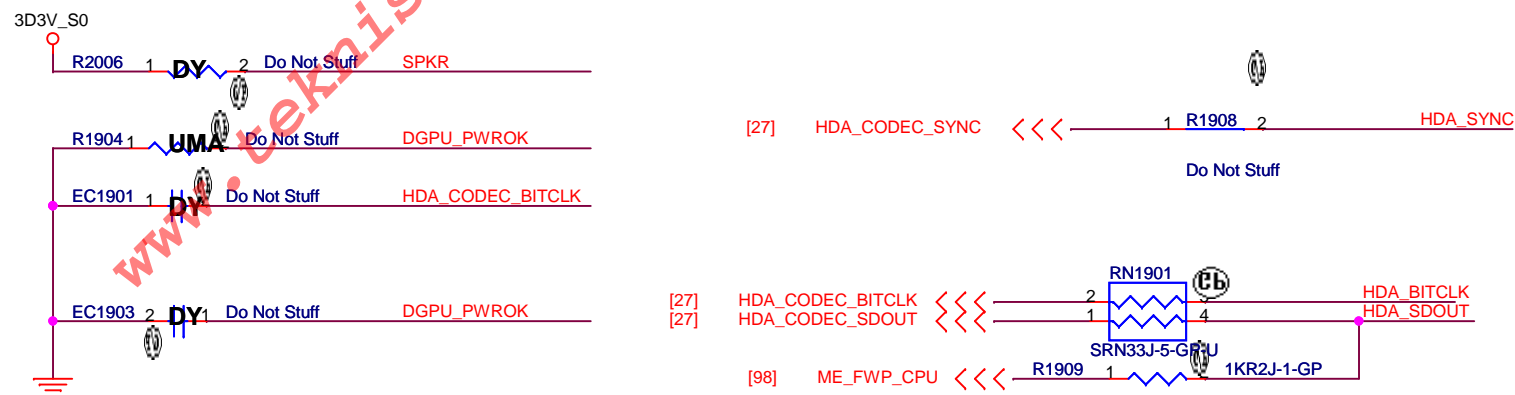
PCH strap pin:

NO REBOOT

HDA_SPKR

* Low = Enable (Default)
High = Disable

The internal pull-down is disabled after
PLTRST# deasserts



2.DIS



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (AUDIO/SDIO/SDXC)

Size
A4

Document Number

Taos KBL-U

Rev
X00

Date: Monday, December 26, 2016

Sheet 19 of 105

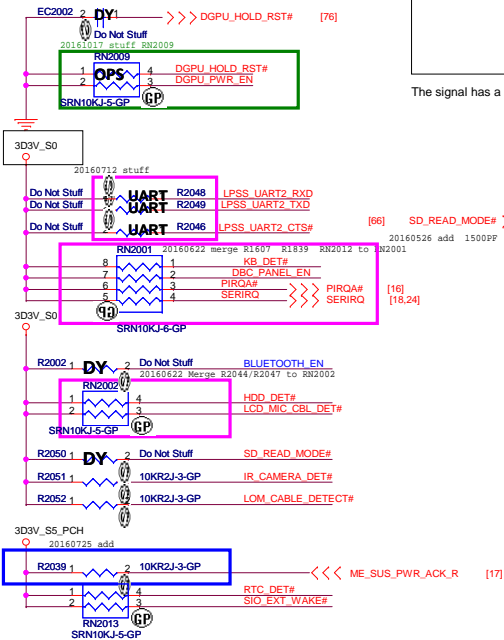
Main Func = PCH

PCH strap pin:

No Reboot	Sampled at rising edge of PCH_PWROK						
GSP1_MOSI / GPP_B22	This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.						
	<table border="0"> <tr> <td>Bit 10</td><td>Boot BIOS Destination</td></tr> <tr> <td>0</td><td>SPI</td></tr> <tr> <td>1</td><td>LPC</td></tr> </table>	Bit 10	Boot BIOS Destination	0	SPI	1	LPC
Bit 10	Boot BIOS Destination						
0	SPI						
1	LPC						

The signal has a weak internal pull-down.

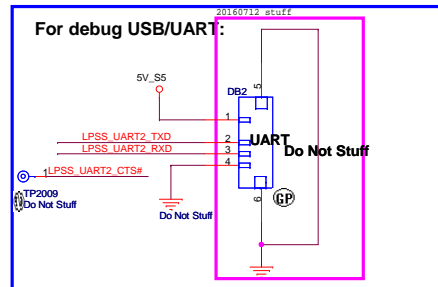
(PDG#543016) Ensure that all I2C interface on-board terminations are pulled up to the same voltage rail as the device/end point.



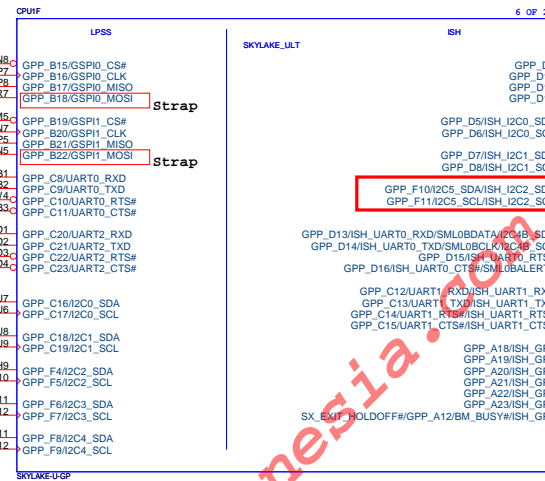
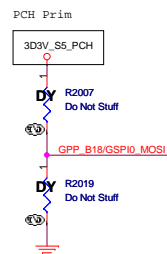
PCH strap pin:

No Reboot	Sampled at rising edge of PCH_PWROK
GSPi0_MOSI / GPP_B18	<p>0 = Disable "No Reboot" mode.</p> <p>1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.</p>

The signal has a weak internal pull-down.

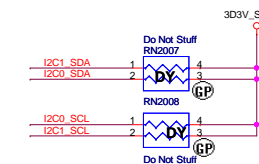


Intel has removed EHCI controller from BDW
and proposed to use UART interface for Win7 debug.



BIOS strap pin:

BIOS VRAM Size Strap pin	PROJECT_ID2
KBL	0
SKL	1



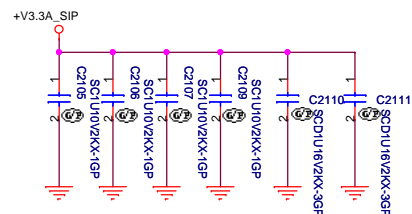
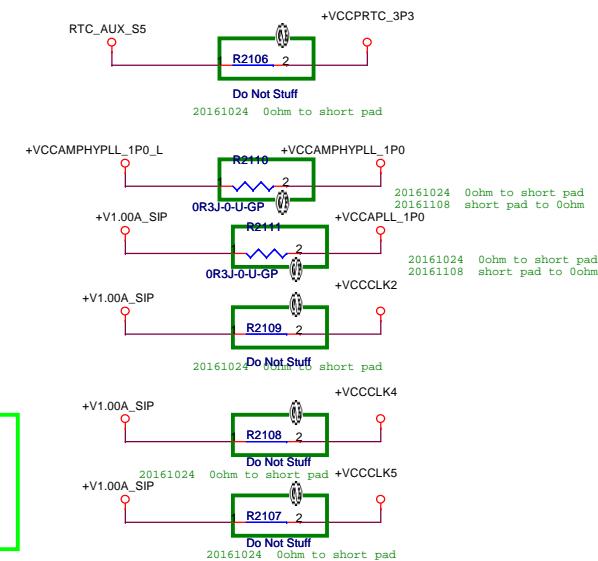
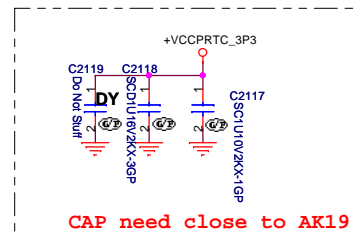
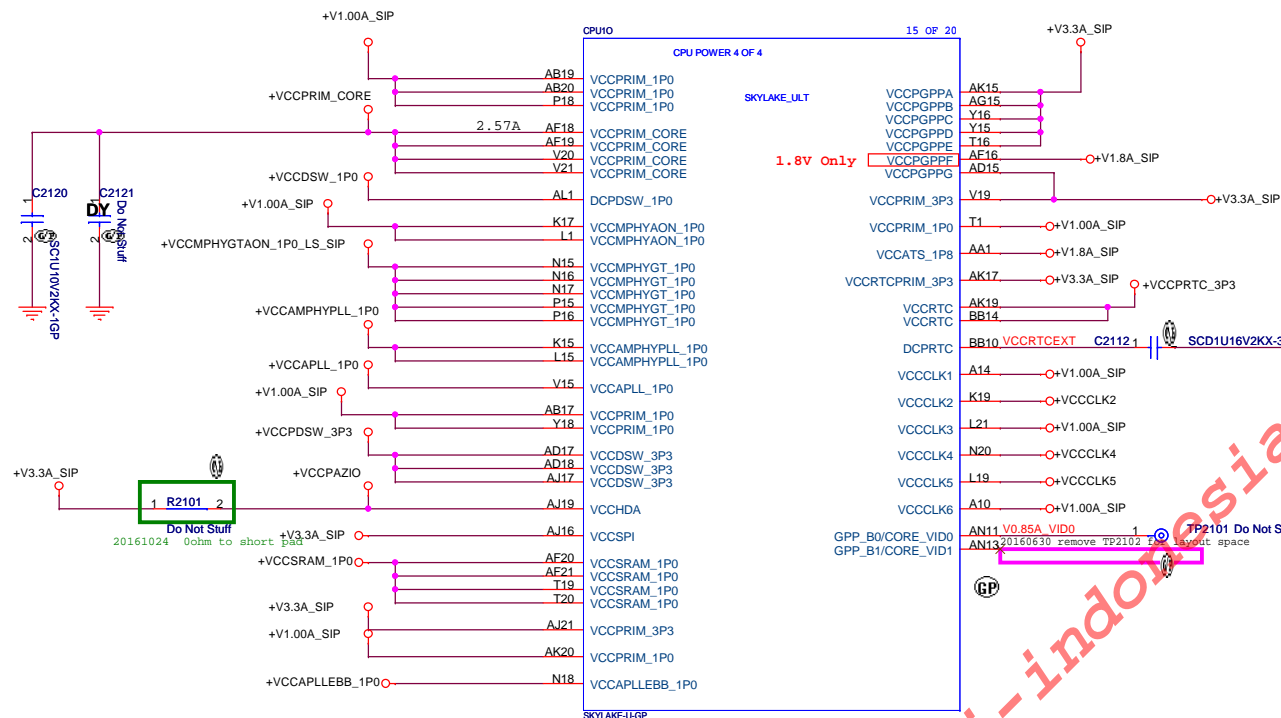
BIOS strap pin:

BIOS UMA/DIS Strap pin	BOARD_ID2
UMA	0
DIS	1

BIOS strap pin:

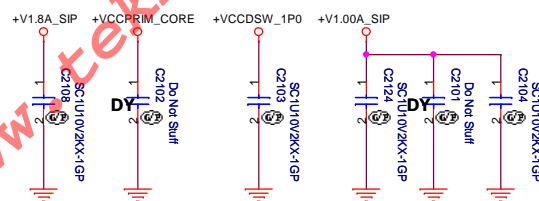
BIOS VRAM Size Strap pin	VRAM_ID1
4G	0
2G	1

Main Func = PCH



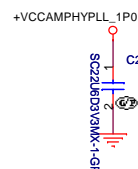
Layout Note:

1uF:
C2105 near V19
C2106 near AK17
C2107 near AG15
C2109 near Y16
C2110 near T16
C2111 near AJ19

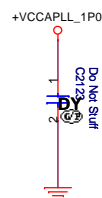


Layout Note:

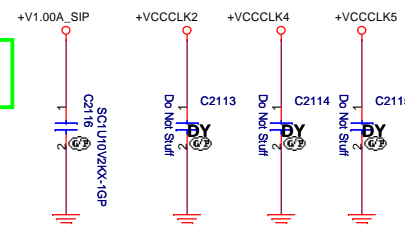
1uF:
C2101 near AB19
C2104 near K17
C2116 near A10
C2124 near AL1



Layout Note:
22uF:
C2122 near K15



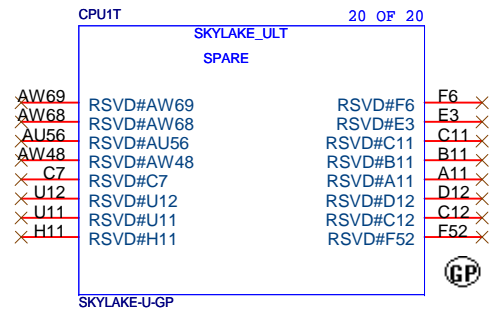
Layout Note:
22uF:
C2123 near K15



Layout Note:


1uF:
C2116 near A10
22uF:
C2115 near K19
C2114 near N20
C2113 near L19

Main Func = PCH

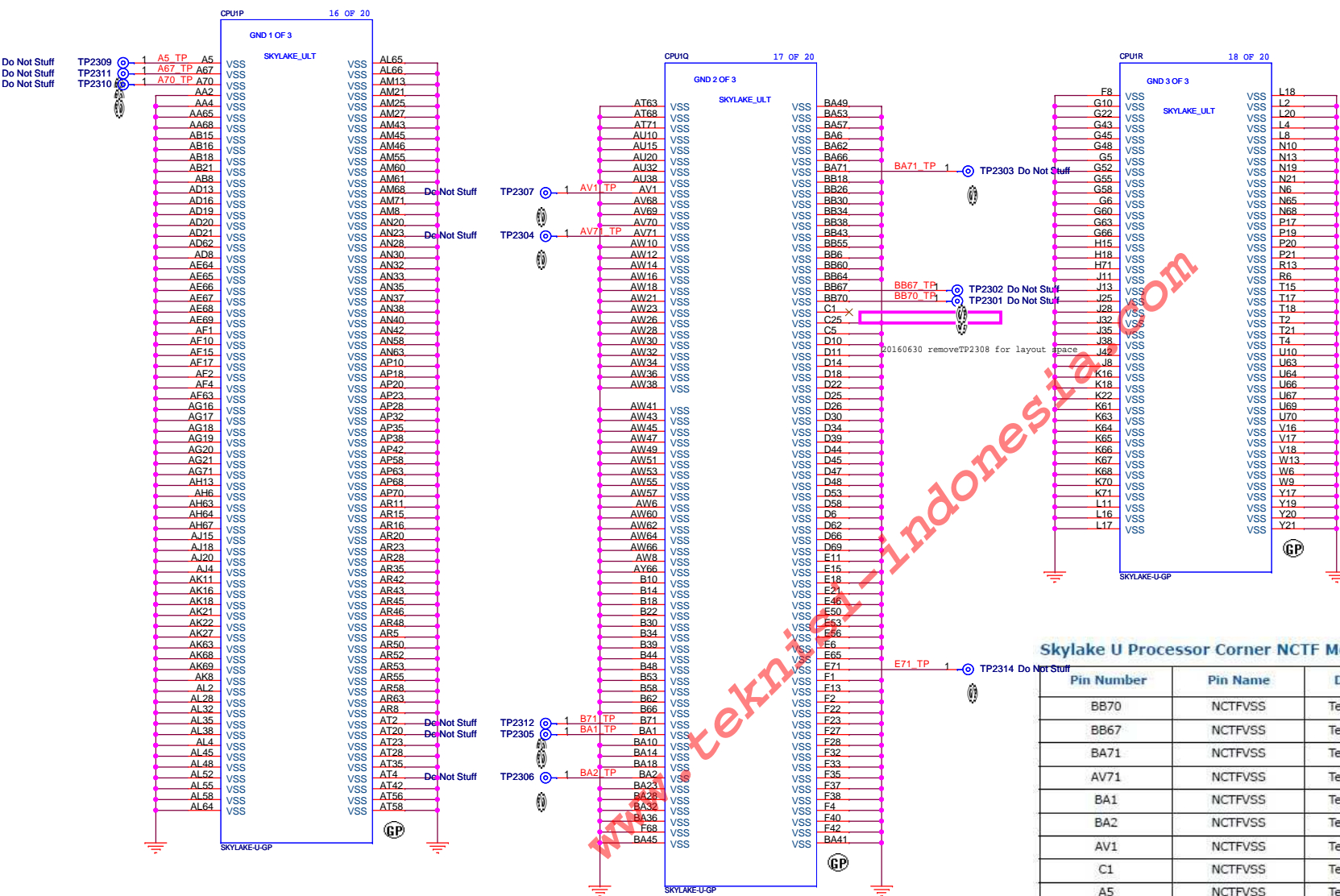


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2.DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CPU (RSVD)			
Size A4	Document Number Taos KBL-U		Rev X00
Date: Monday, December 26, 2016		Sheet 22 of	105


Main Func = PCH



Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	Corner BB1
BA1	NCTFVSS	Test Point (TP)	
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	Corner A1
C1	NCTFVSS	Test Point (TP)	
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

2.DIS



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (VSS)

Size

A3

Document Number

Taos KBL-U

Rev

X00

Date:

Monday, December 26, 2016

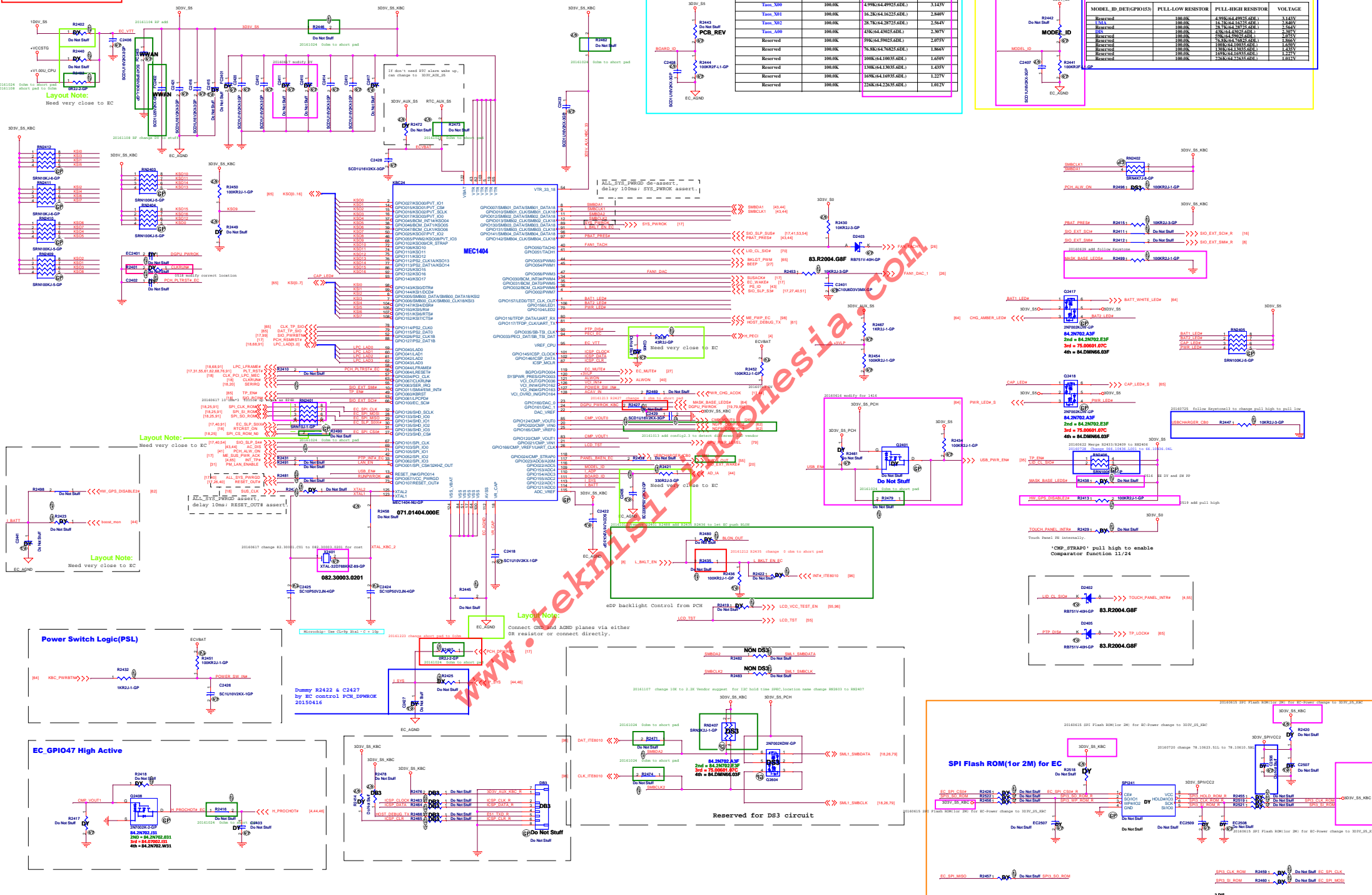
Sheet

23

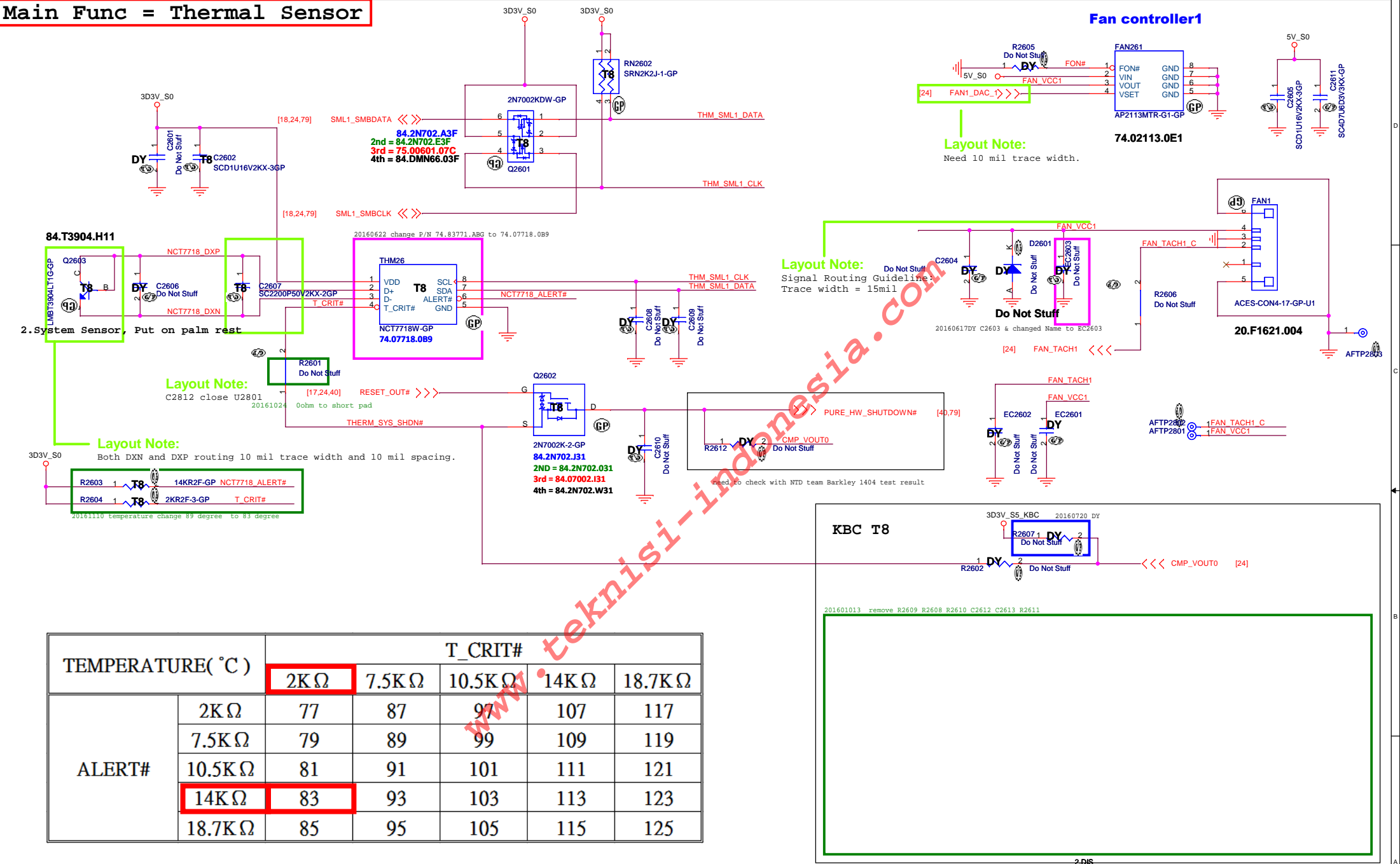
of

105

Main Func = KBC

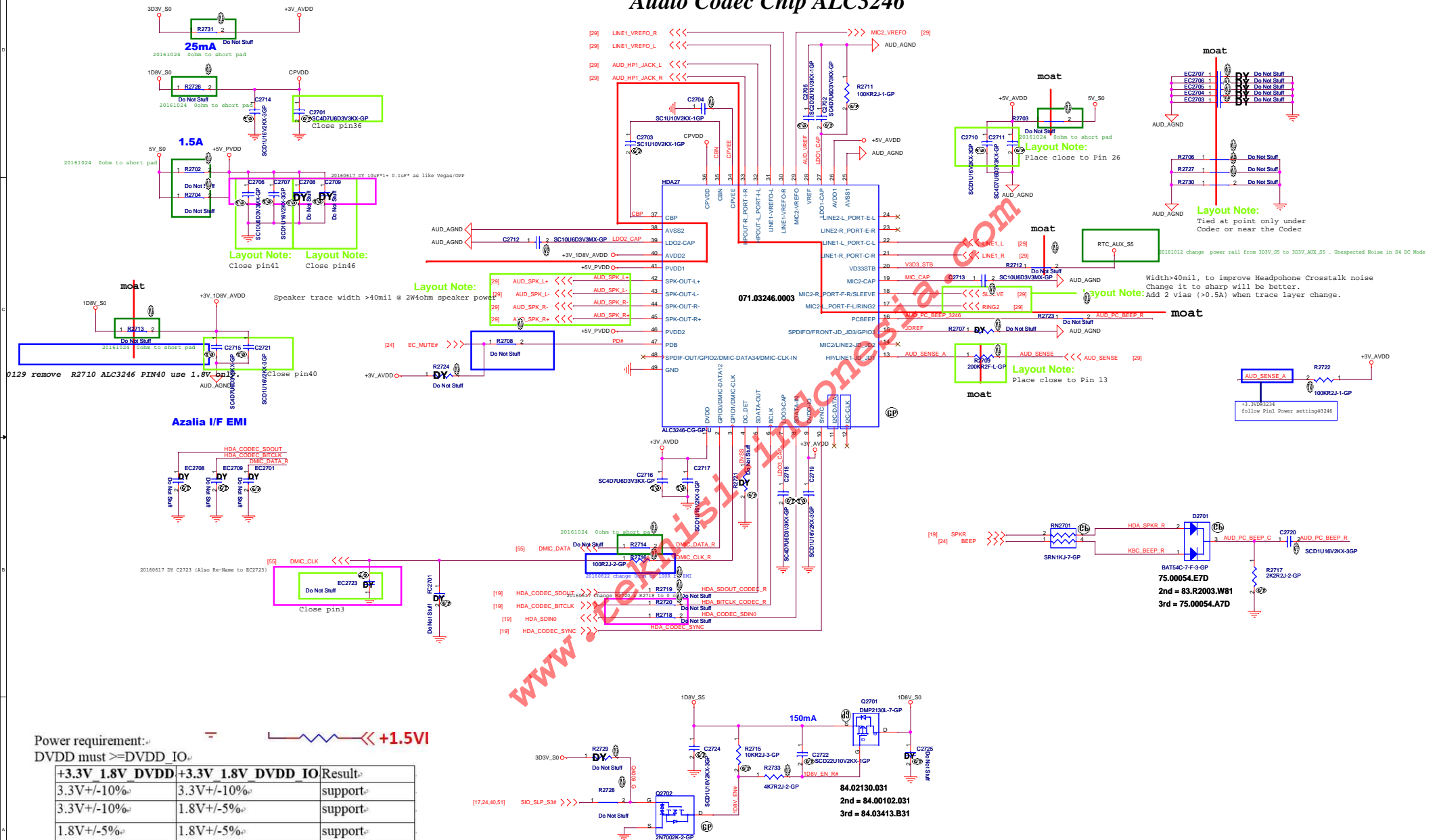


Main Func = Thermal Sensor



TEMPERATURE(°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

Audio Codec Chip ALC3246




Power requirement:
DVDD must >= DVDD_IO

+3.3V	1.8V	DVDD	+3.3V	1.8V	DVDD	IO	Result
3.3V+/-10%	3.3V+/-10%		3.3V+/-10%				support
3.3V+/-10%			1.8V+/-5%				support
1.8V+/-5%			1.8V+/-5%				support
1.8V+/-5%			1.5V+/-5%				support
1.8V+/-5%			3.3V+/-10%				Not support

(Blanking)

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2.DIS

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Title (Reserved)			
Size A4	Document Number Taos KBL-U		Rev X00
Date: Monday, December 26, 2016		Sheet 28 of	105

Main Func = Audio

(Blanking)

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2.DIS



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size
A4

Document Number

Taos KBL-U

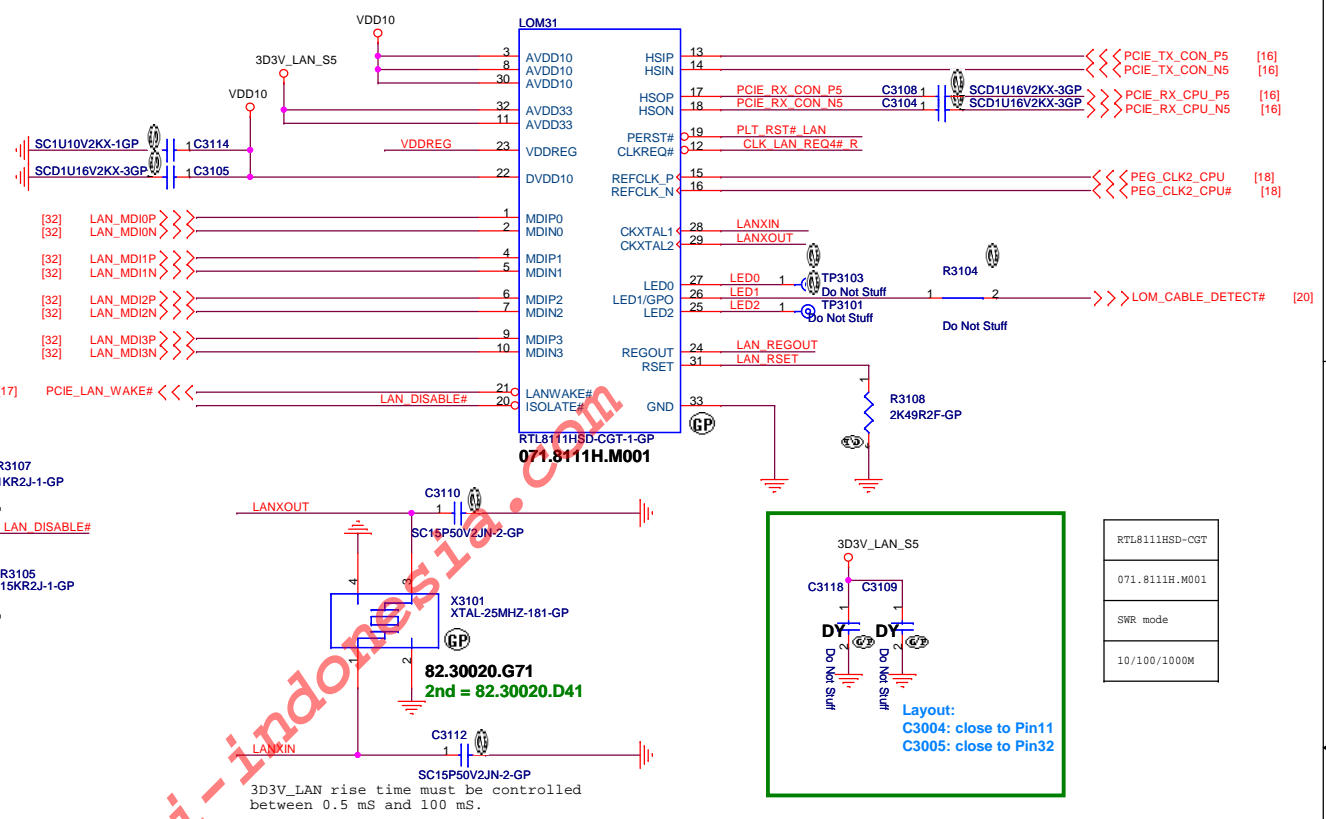
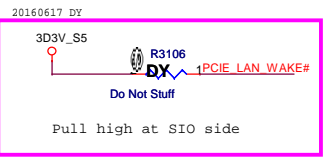
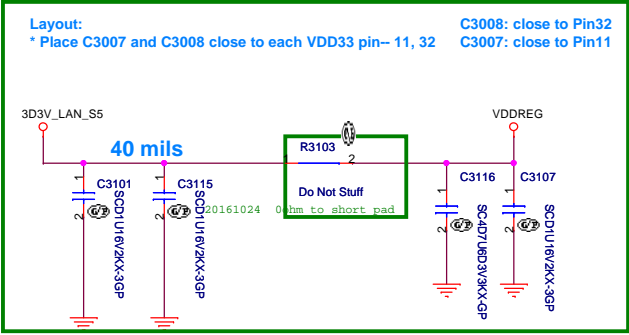
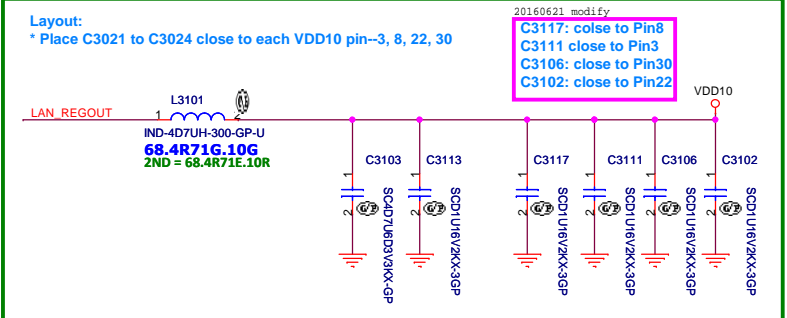
Rev

X00

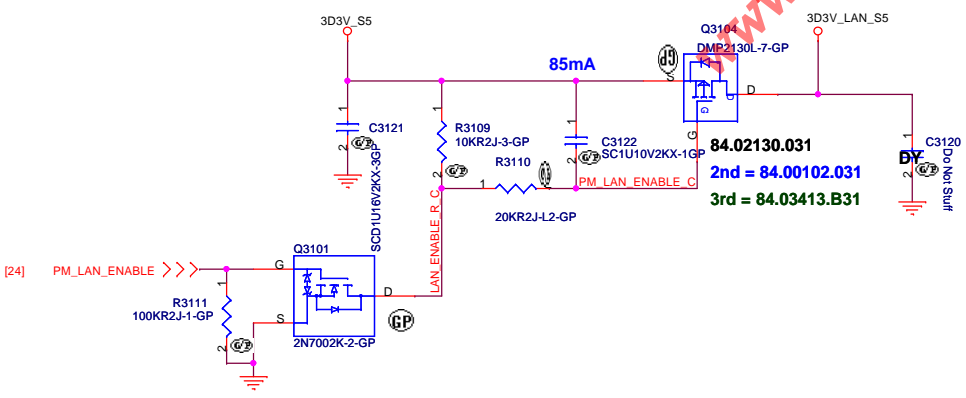
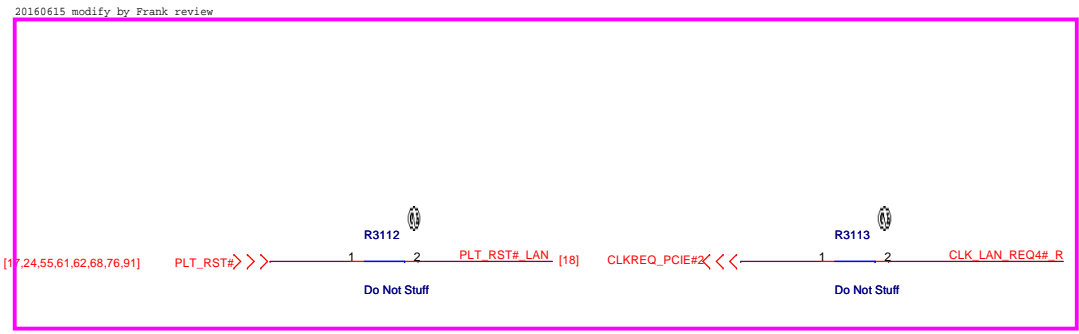
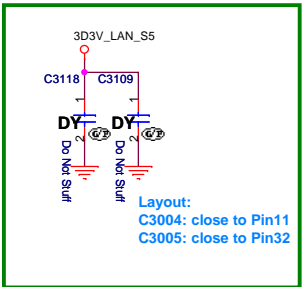
Date: Monday, December 26, 2016

Sheet 30 of 105

Main Func = LAN



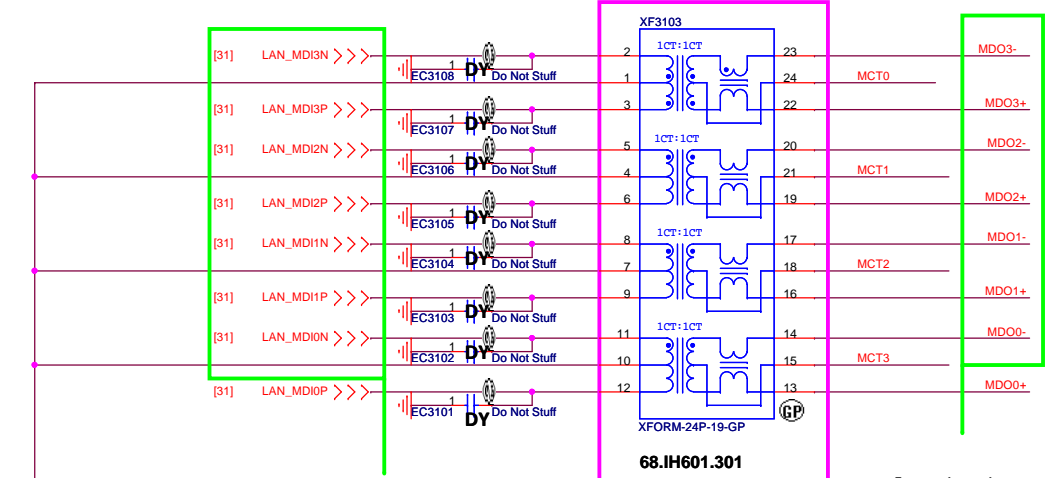
RTL8111HSD-CGT
071.8111H.M001
SWR mode
10/100/1000M



Main Func = LAN

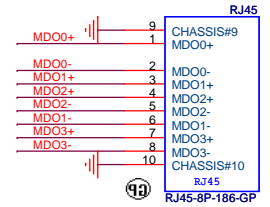
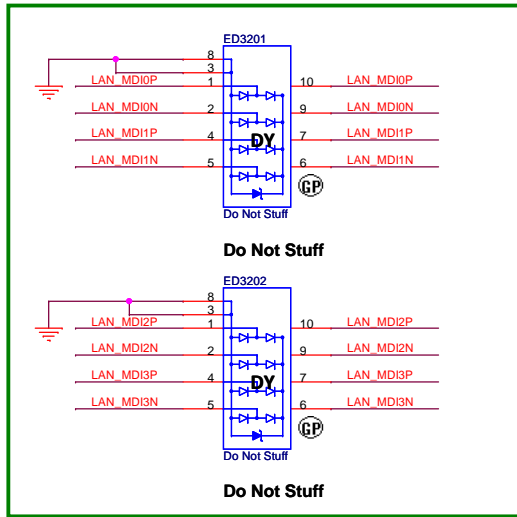
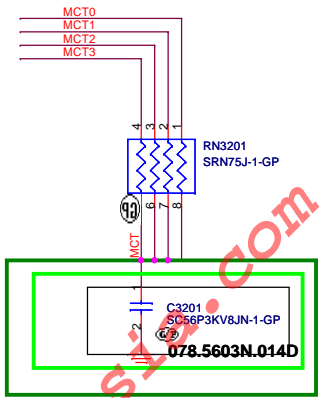
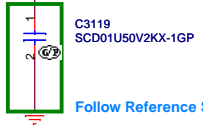
LAN TransFormer (10/100/1000M)

20160706 change P/N 068.IH219.3001 to 68.IH601.301 because EMI fail



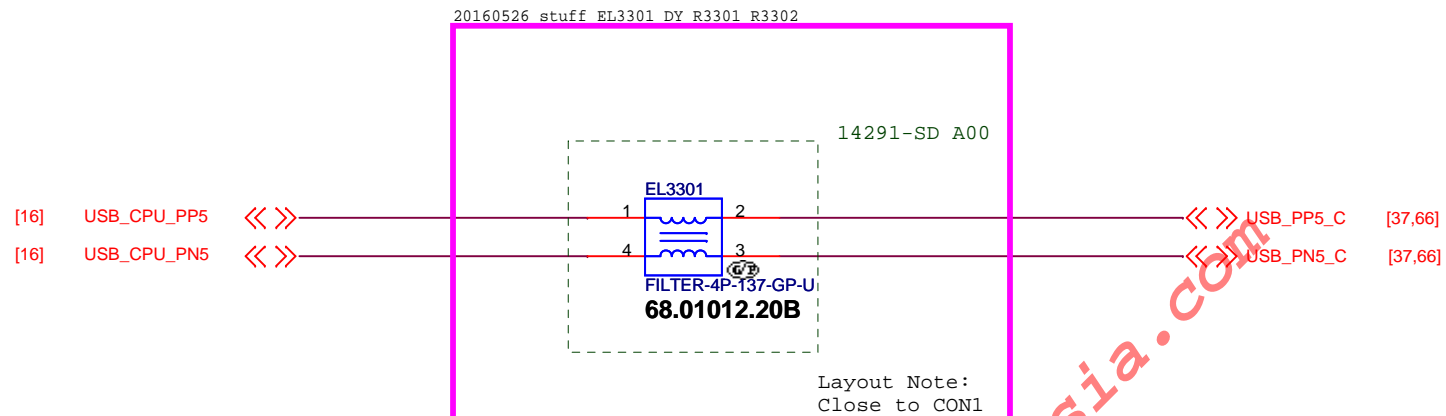
Layout note:
30 mil spacing between MDI differential pairs.

Layout note:
30 mil spacing between MDI differential pairs.



022.10001.0D41
RJ45
Main : 022.10001.0D41
2nd : 022.10001.0C41

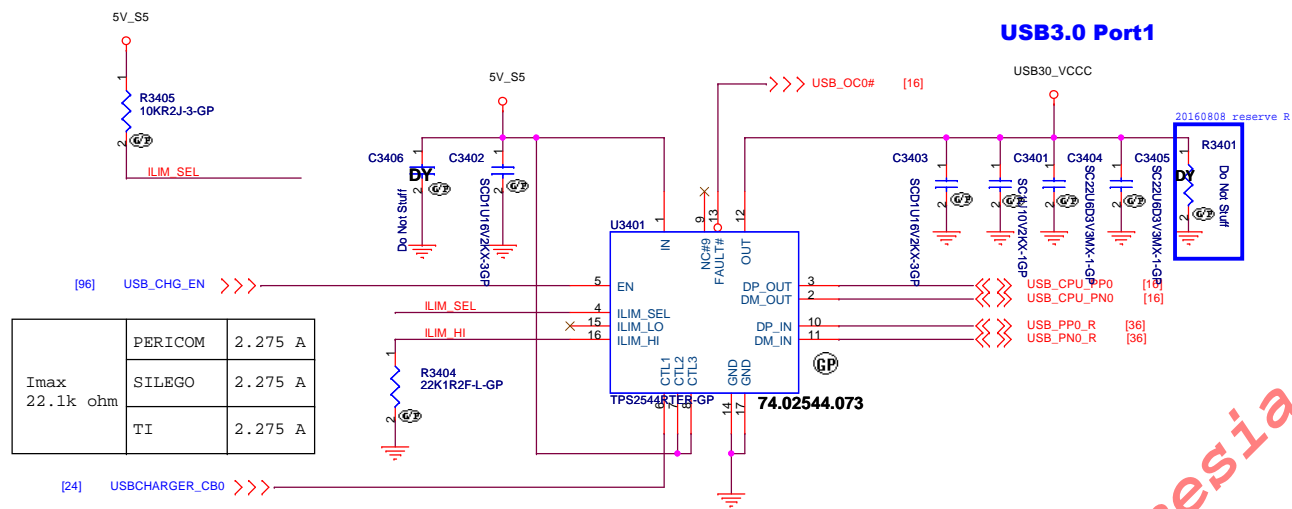
Main Func = Card Reader



2.DIS

DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Card Reader-RTS5170			
Size A4	Document Number Taos KBL-U		Rev X00
Date: Monday, December 26, 2016		Sheet 33 of	105

Main Func = USB2.0 Port3



PI5USB2544 Device Control Pins Truth Table

CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Comment
0	0	0	0	Discharge	NA	OUT held low
0	0	0	1	Discharge	NA	OUT held low
0	x	1	x	DCP_Auto	ILIM_HI	Data lines disconnected
0	1	0	0	SDP1	ILIM_LO	Data lines connected
0	1	0	1	SDP1	ILIM_HI	Data lines connected
0	1	1	0	DCP_Auto	ILIM_HI	Data lines disconnected
0	1	1	1	DCP_Auto	ILIM_HI	Data lines disconnected
1	0	0	0	DCP_Shorted	ILIM_LO	Device forced to stay in DCP BC1.2 charging mode
1	0	0	1	DCP_Shorted	ILIM_HI	Device forced to stay in DCP BC1.2 charging mode
1	0	1	0	Divider-1A	ILIM_LO	Device forced to stay in Divider-1A charging mode
1	0	1	1	Divider-1A	ILIM_HI	Device forced to stay in Divider-1A charging mode
1	1	0	0	SDP1	ILIM_LO	Data lines connected
1	1	0	1	SDP1	ILIM_HI	Data lines connected
1	1	1	0	SDP2 ⁽¹⁾	ILIM_LO	Data lines connected
1	1	1	1	CDP ⁽¹⁾	ILIM_HI	Data lines connected

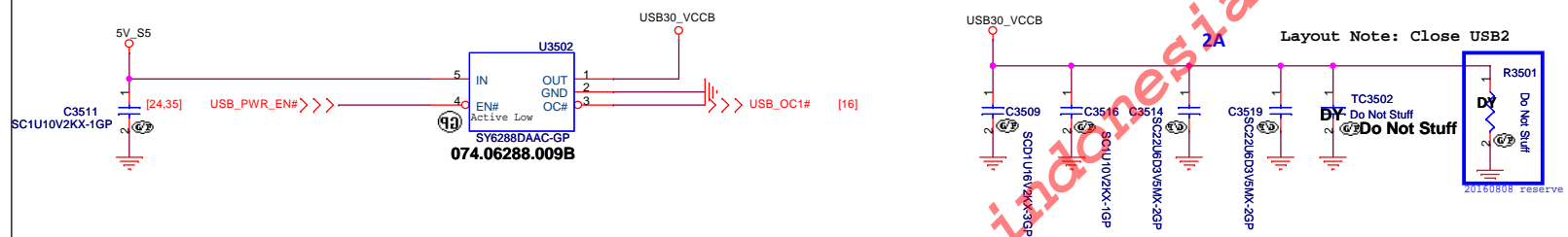
Note:
(1) No OUT discharge when changing between 1111 and 1110.

Main Func = USB3.0 Port1

USB3.0 Port1

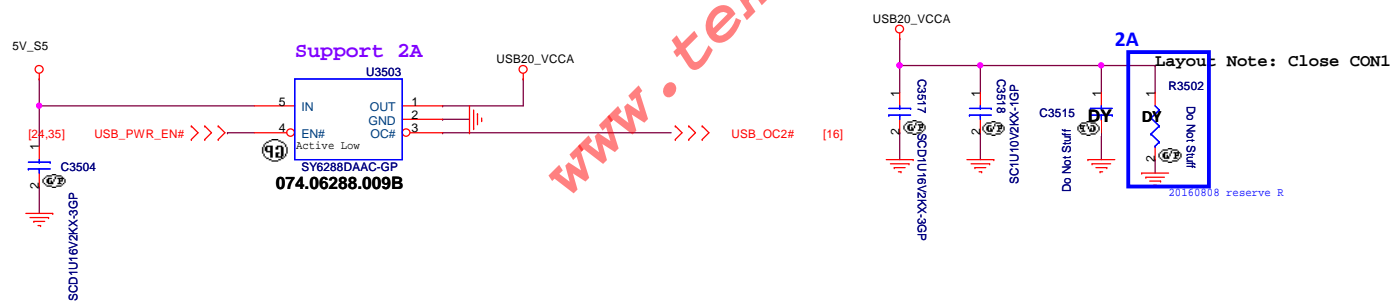
Main Func = USB3.0 Port2

USB3.0 Port2



Main Func = USB2.0 Port3

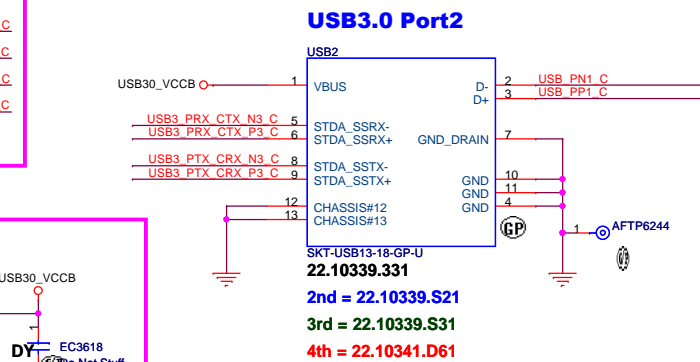
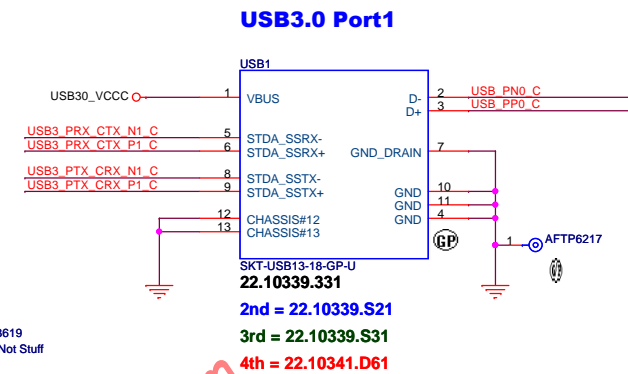
USB2.0 Port3 (IO Board)



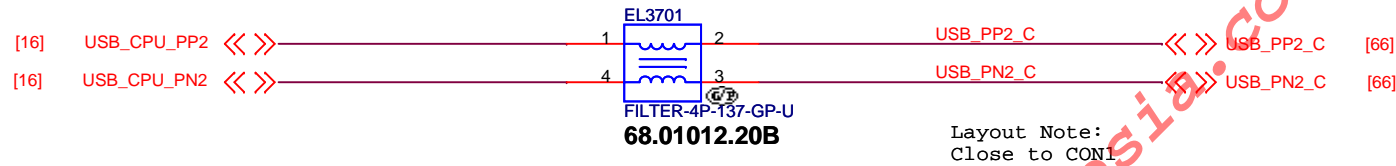
2.DIS



Title			USB switch	
Size	Document Number	Rev	X00	
Date: Monday, December 26, 2016			Sheet 35	of 105



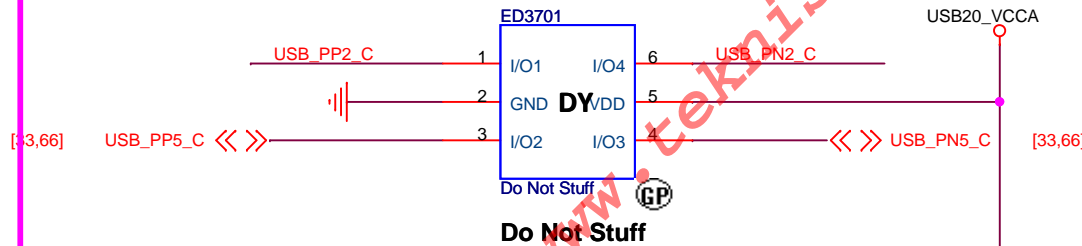
USB3 (USB2.0) CMC



20160615 DY ED3701 by EMI

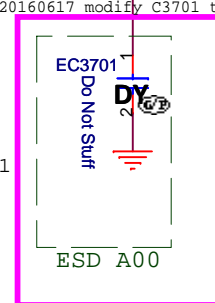
USB ESD Diode

Stuff for ESD R2 spec



20160617 modify C3701 to EC3701 and DY

Layout Note:
Close to CON1



2.DIS


DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title USB20			
Size A4	Document Number Taos KBL-U		Rev X00
Date: Monday, December 26, 2016		Sheet 37 of 105	

Main Func = USB3.0 Port1

(Blanking)

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2.DIS


		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number Taos KBL-U		Rev X00
Date: Monday, December 26, 2016		Sheet 38 of	105

Main Func = USB3.0 Port1

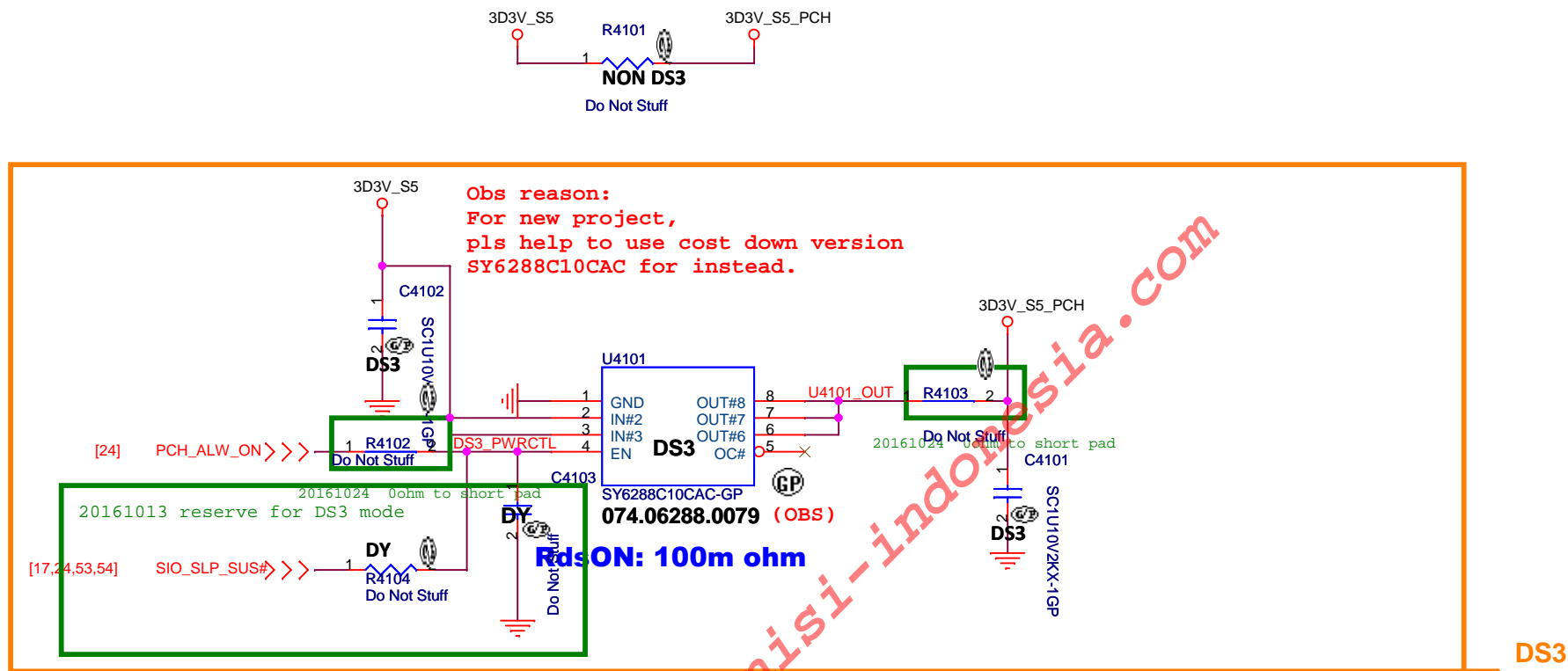
(Blanking)

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2.DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number Taos KBL-U		Rev X00
Date: Monday, December 26, 2016		Sheet 39 of	105

Main Func = Power Plane & Sequence



2.D/S


DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Connected_Standby(1/2)+DS3			
Size A4	Document Number Taos KBL-U		Rev X00
Date: Monday, December 26, 2016		Sheet 41 of	105

Main Func = DIMM1
Main Func = DIMM2

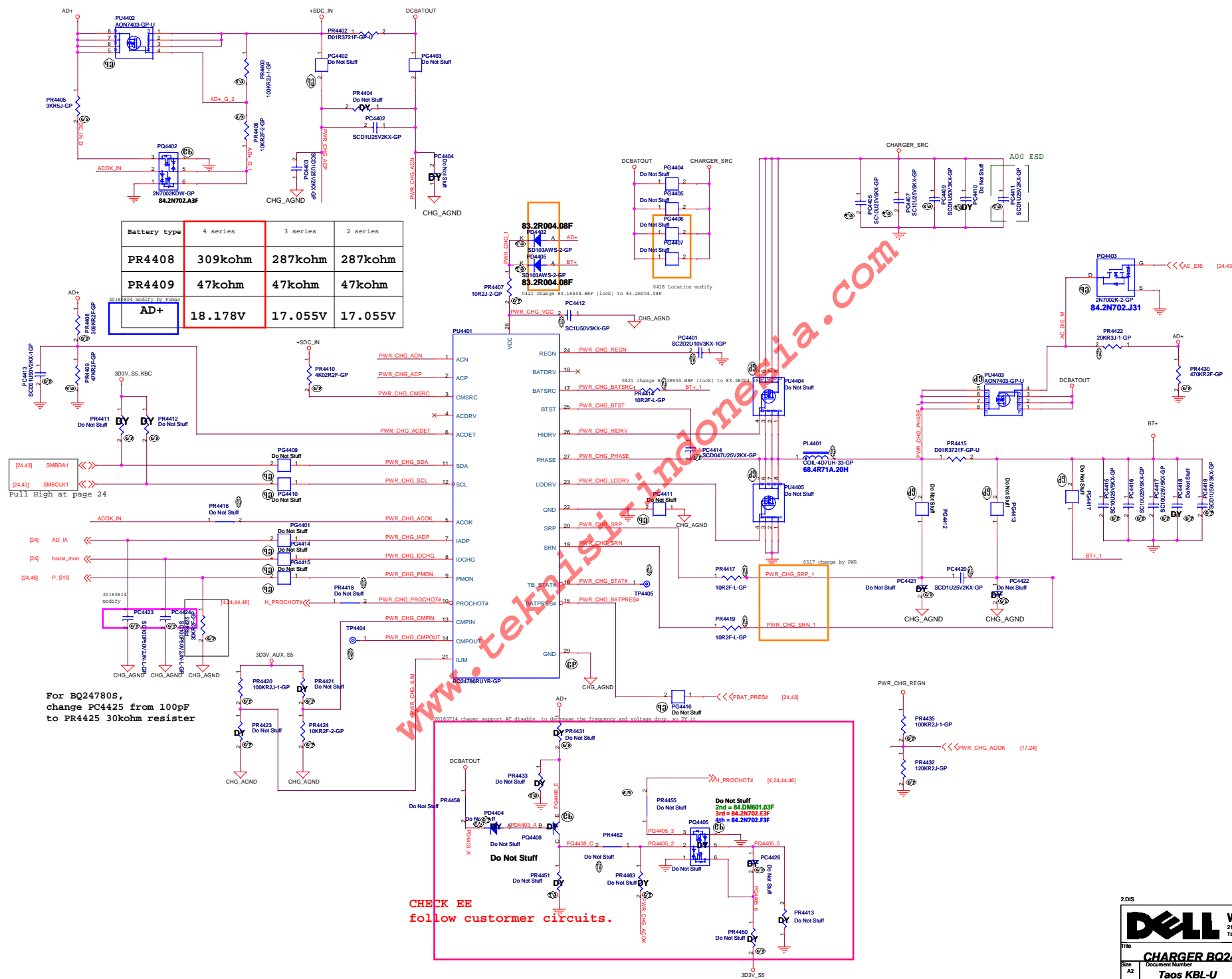
VREF CIRCUITRY

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2.DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Connected_Standby(2/2)			
Size A4	Document Number Taos KBL-U		Rev X00
Date: Monday, December 26, 2016		Sheet 42 of	105

Main Func = Charger



	U22 15W	U23a 28W
PR4637	47K (64.47025, 55L)	73K (64.73225, 55L)
PR4641	47K (64.47025, 55L)	73K (64.73225, 55L)
PR4640	12.4K (64.12425, 60L)	15K (64.15025, 60L)
PR4662	69.9K (64.69925, 60L)	88.7K (64.88725, 60L)
PR4658	88.7K (64.88725, 60L)	90.9K (64.90925, 60L)
PR4647	2.37K (64.23715, 60L)	2.15K (64.21515, 60L)
PR4635	18.3K (64.38325, 60L)	37.4K (64.37425, 60L)
PR4628	73.2K (64.73225, 60L)	69.8K (64.69825, 60L)

NTC-100K-11-GP-U
69.60013.201

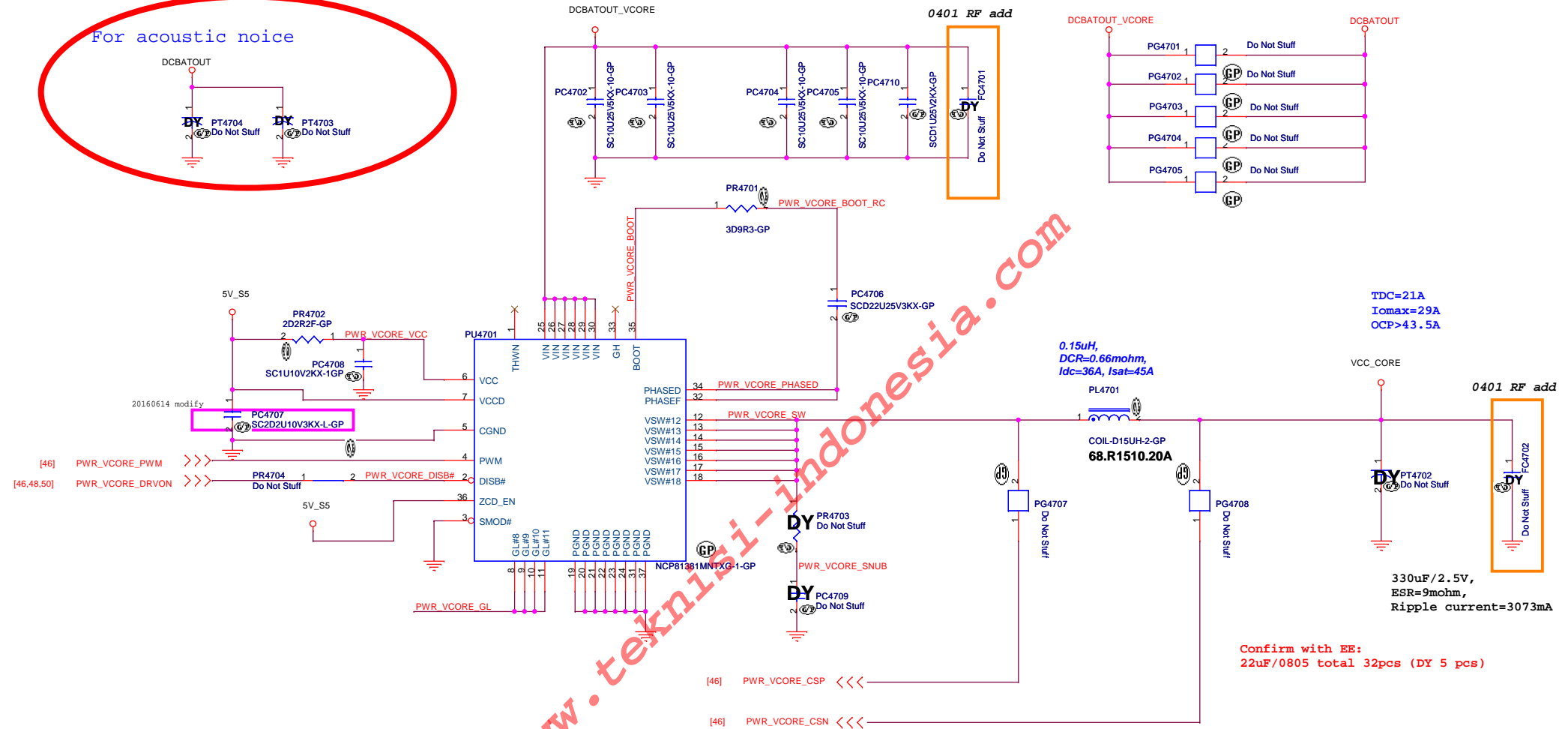
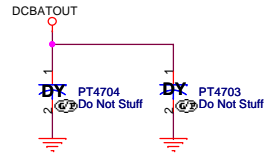
www.Indonesia.com

For NCP81208MNTXG-2-GP Vboot

2.0S

Main Func = CPU_CORE

For acoustic noise



TDC=21A
I_omax=29A
OCP>43.5A

Confirm with EE:
22uF/0805 total 32pcs (DY 5 pcs)

2.DIS

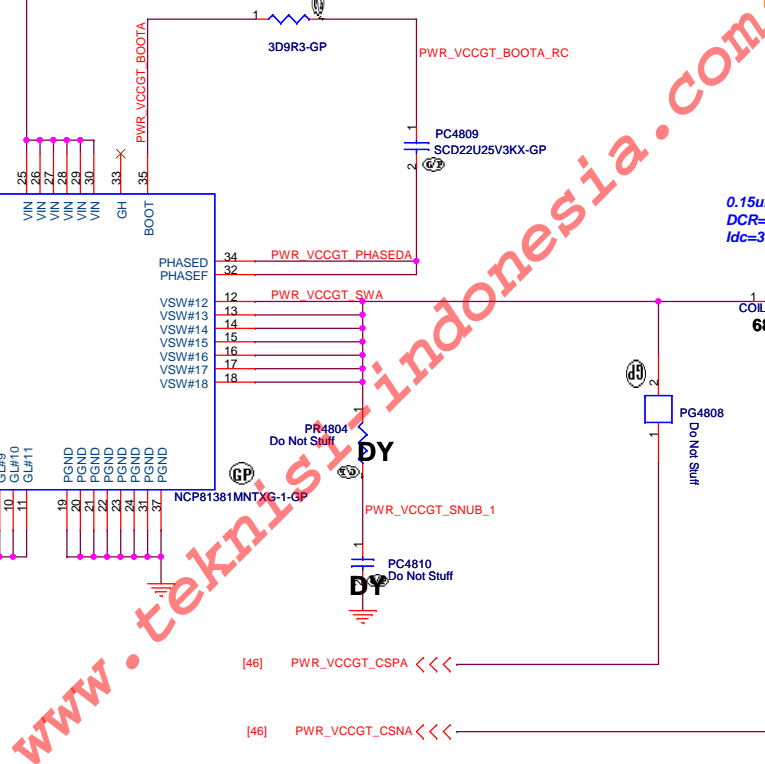
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.


Title
NCP81382MN_CPU_VCORE(2/3)


Size A3 Document Number **Taos KBL-U** Rev **X00**

Date: Monday, December 26, 2016 Sheet 47 of 105


```
Main Func = CPU_CORE
```



		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title NCP81382MN_CPU_VCCGT(3/3)			
Size A3	Document Number Taos KBL-U	Rev X00	
Date:	Monday, December 26, 2016	Sheet 48 of	105


		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title NCP81382MN_CPU_VCCGT(3/3)			
Size A3	Document Number Taos KBL-U	Rev X00	
Date:	Monday, December 26, 2016	Sheet 48	of 105

Main Func = CPU_CORE

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2.DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title NCP81210MN_CPU_VCCGTUS		
Size A4	Document Number Taos KBL-U	Rev X00
Date: Monday, December 26, 2016		Sheet 49 of 105

Main Func = VDDQ

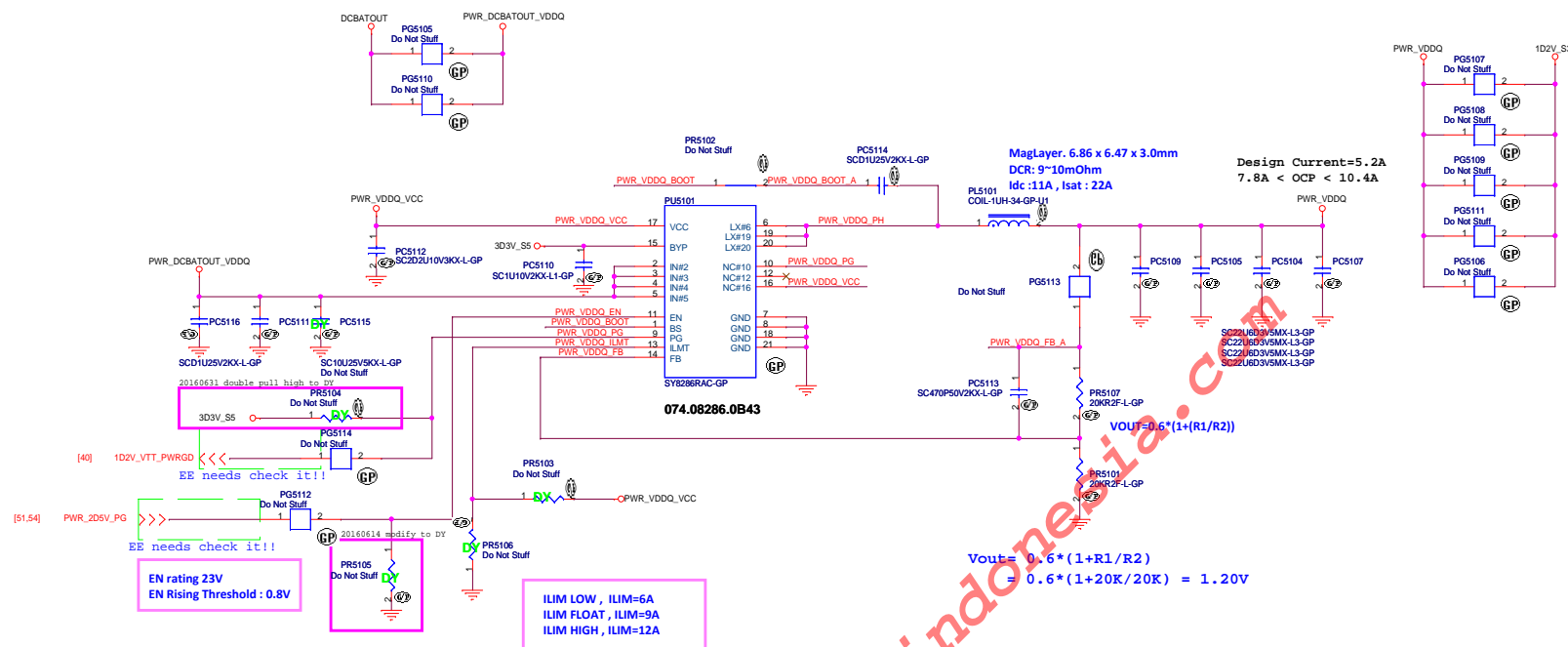
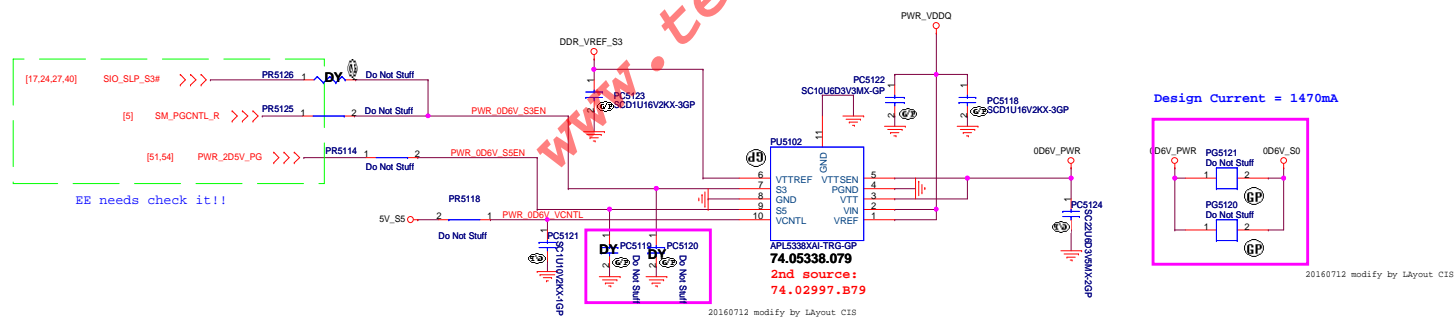



Table1. The Truth Table of S3 and S5 pins

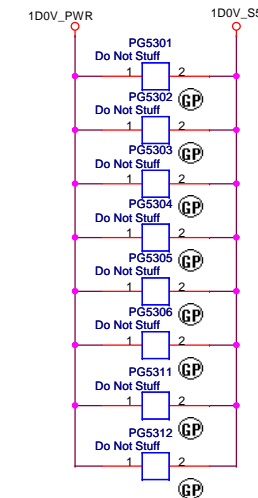
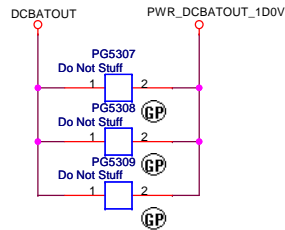
STATE	S3	S5	VDDQ	VTTREF	VTT
S0	H	H	1	1	1
S3	L	H	1	1	0 (high-Z)
S4/5	L	L	0 (discharge)	0 (discharge)	0 (discharge)



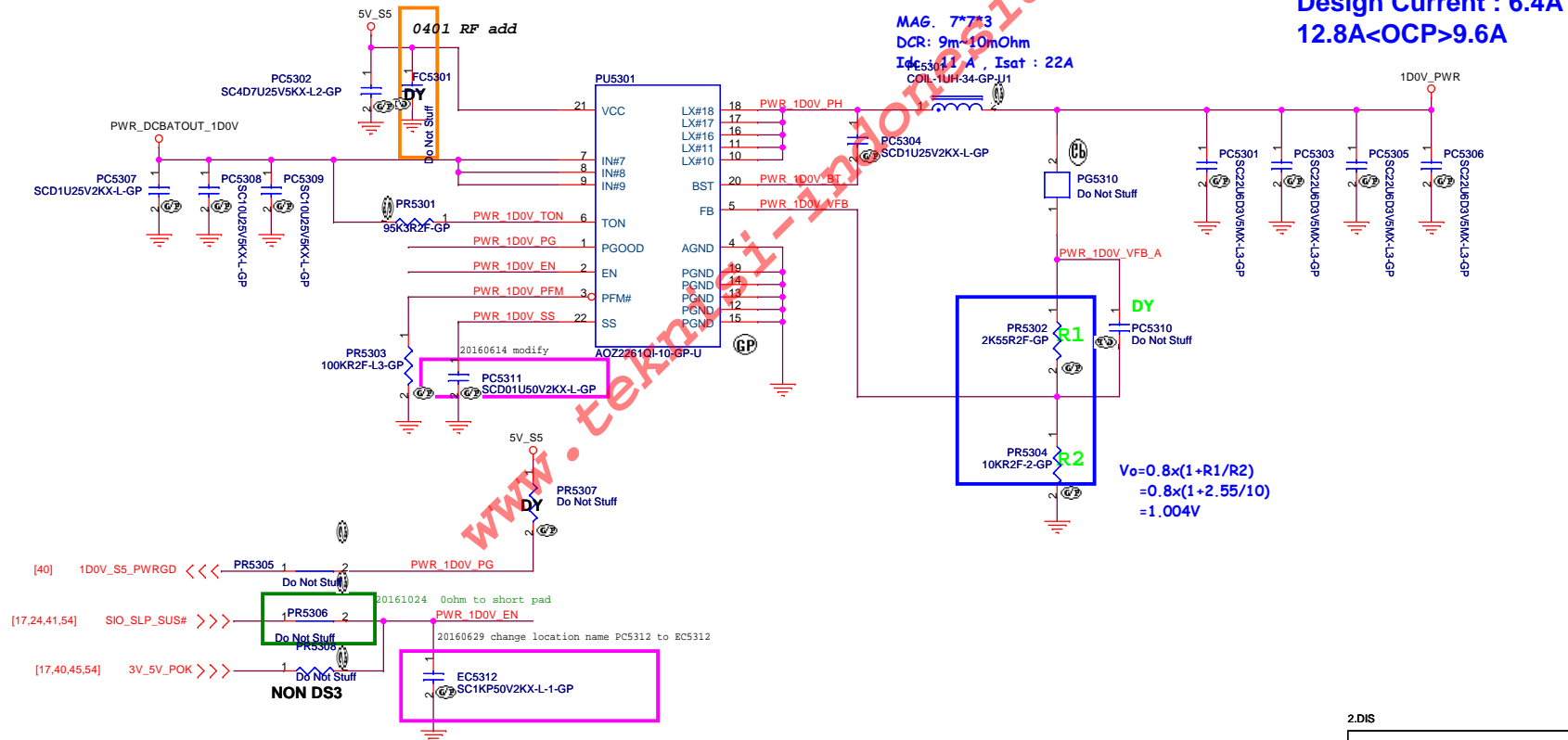
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2.DIS			
		Wistron Corporation 21F, 6th, Sec. 1, Hsin Tai Yiu Rd., Hsichia, Taipei Hsien 221, Taiwan, R.O.C.	
Title DCDC-0D975V_VCCIO			
Size A2	Document Number Taos KBL-U	Rev X00	
Date: Monday, December 26, 2016		Sheet 52 of	106

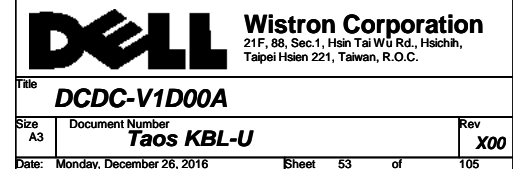
Main Func = 1D0V



AOZ2261 for 1D0V



2.DIS



APL5930 for DDR4_VPP

1230

change VPP_EN to SIO_SLP_S4#

change PWRGD_VPP to PWR_2D5V_PG

NEED EE CHECK

NEED EE CHECK

1230 change P_5V_A to 5V_S5

1230 change P_3.3V_A to 3D3V_S5

Design Current=0.7A

RT9025 for 1D8V_S5

Design Current = 454mA

$$V_{out} = 0.8V * (R1 + R2) / R2$$

2.DIS


DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		LDO-V1D5V&V1D8V	
Size	A3	Document Number	Taos KBL-U
Date:	Monday, December 26, 2016	Sheet	54 of 105
Rev	X00		

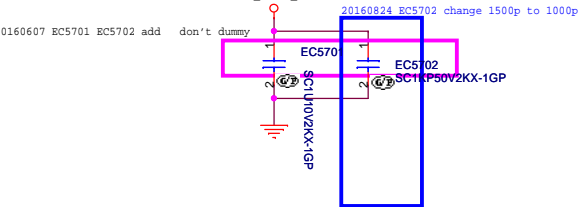
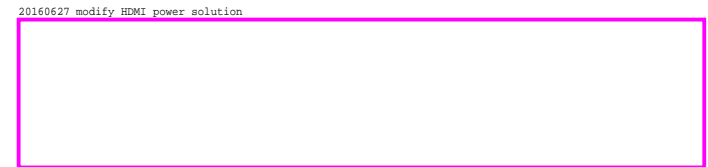
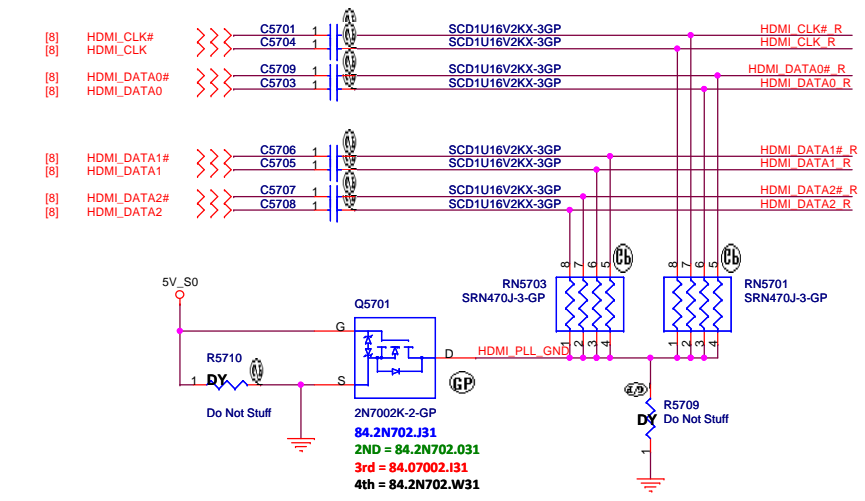
(Blanking)

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2.DIS

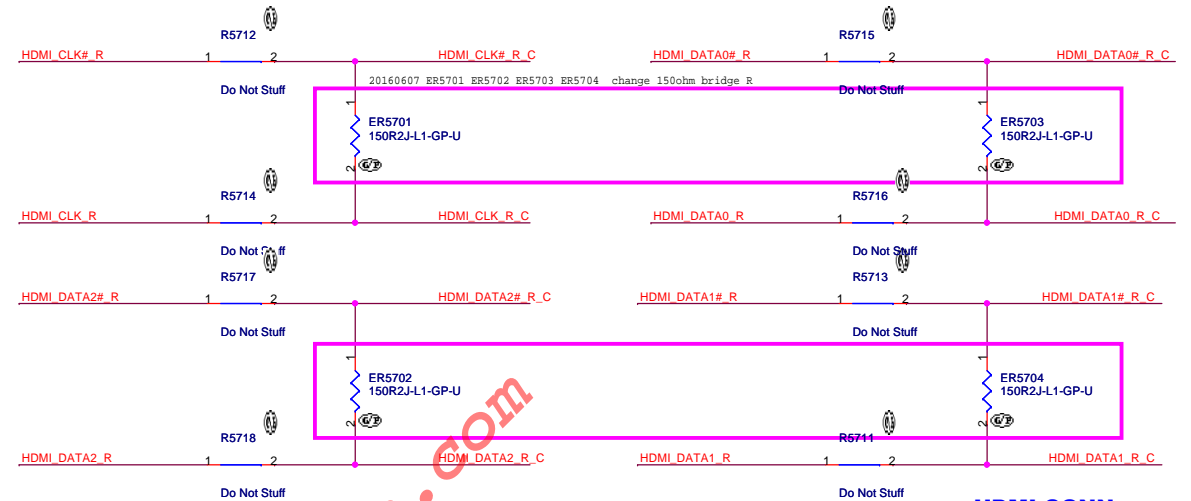
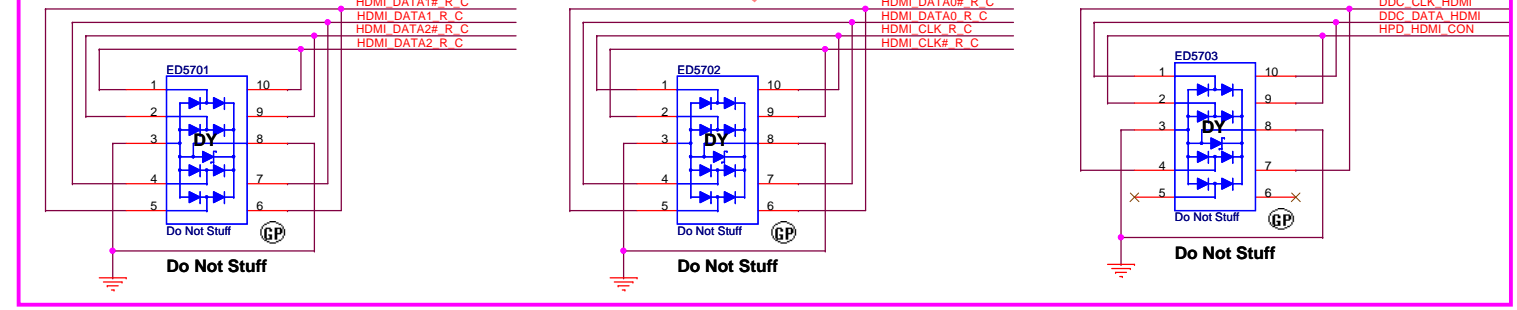
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CRT			
Size A4	Document Number Taos KBL-U		Rev X00
Date: Monday, December 26, 2016		Sheet 56	of 105

Main Func = HDMI

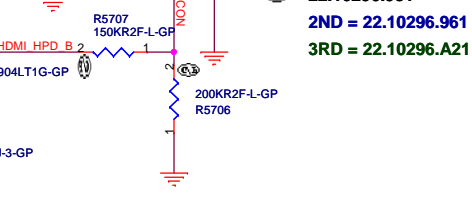
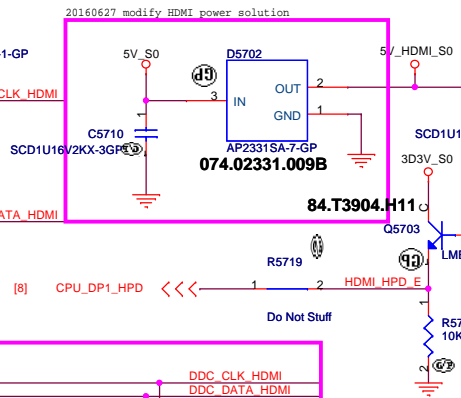
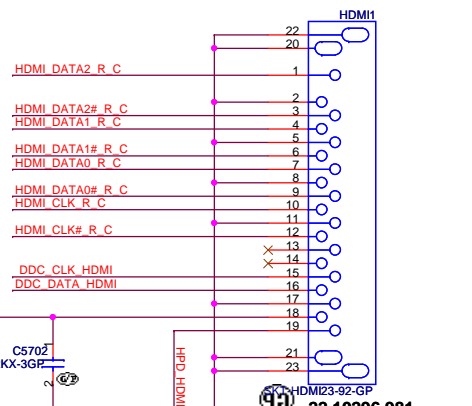


20160615 stuff by EMI
20160623 modify 75.00524.A73 to 75.08808.073
20161018 change stuff to DY by EMI

EMI Request:




HDMI CONN



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2.DIS

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Title (Reserved)		
Size A4	Document Number Taos KBL-U	Rev X00
Date: Monday, December 26, 2016		Sheet 58 of 105

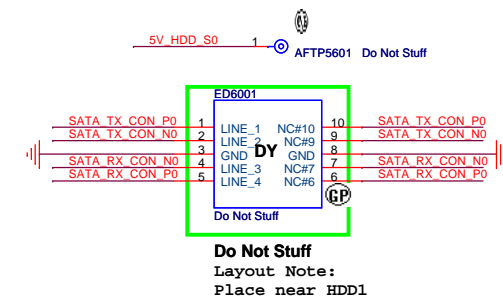
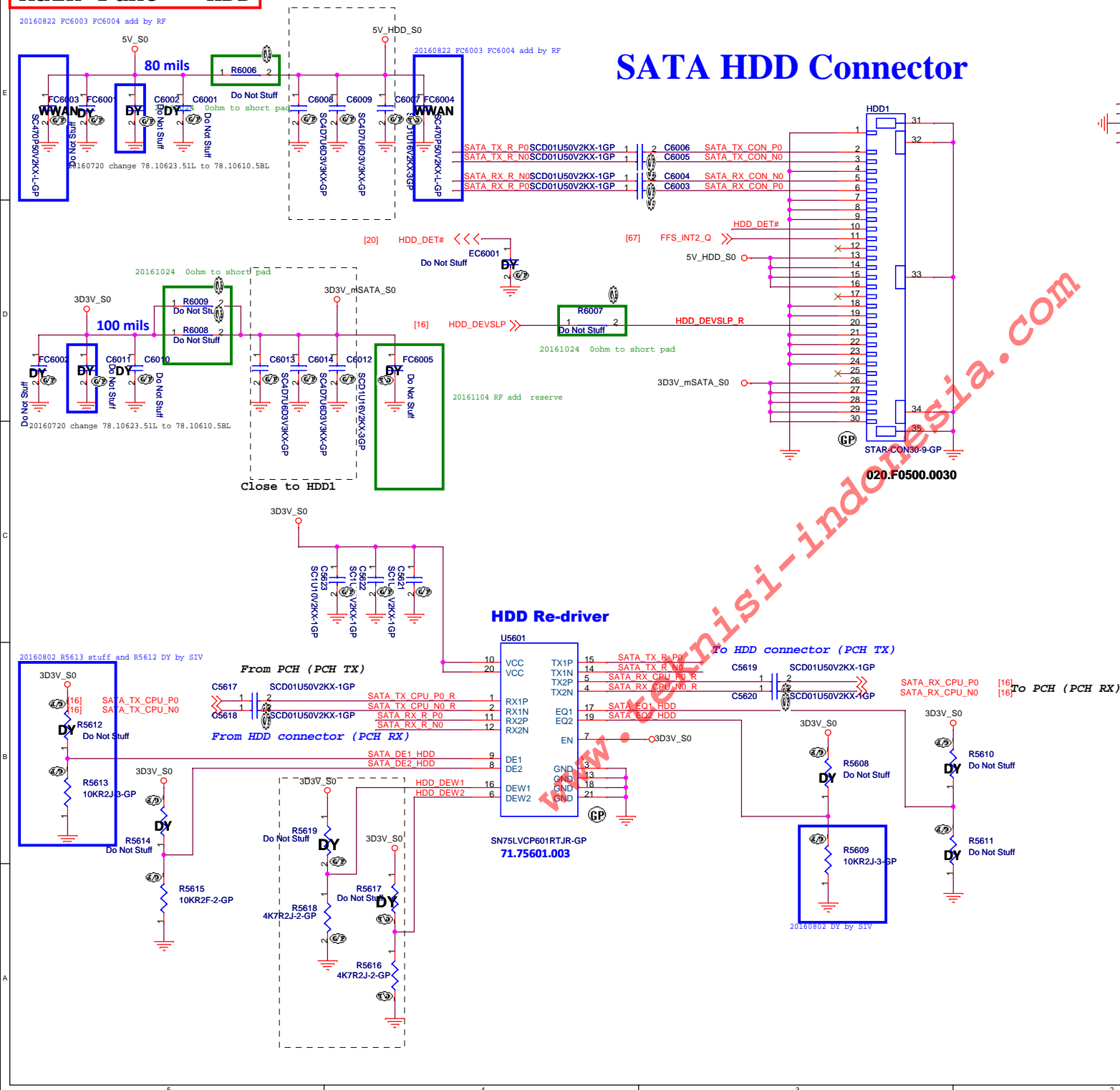
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(Blanking)

2.DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number Taos KBL-U		Rev X00
Date: Monday, December 26, 2016		Sheet 59 of	105

20160822 FC6003 FC6004 add by RF



2.DIS



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
Title																													

SATA HDDSize
A3

Document Number

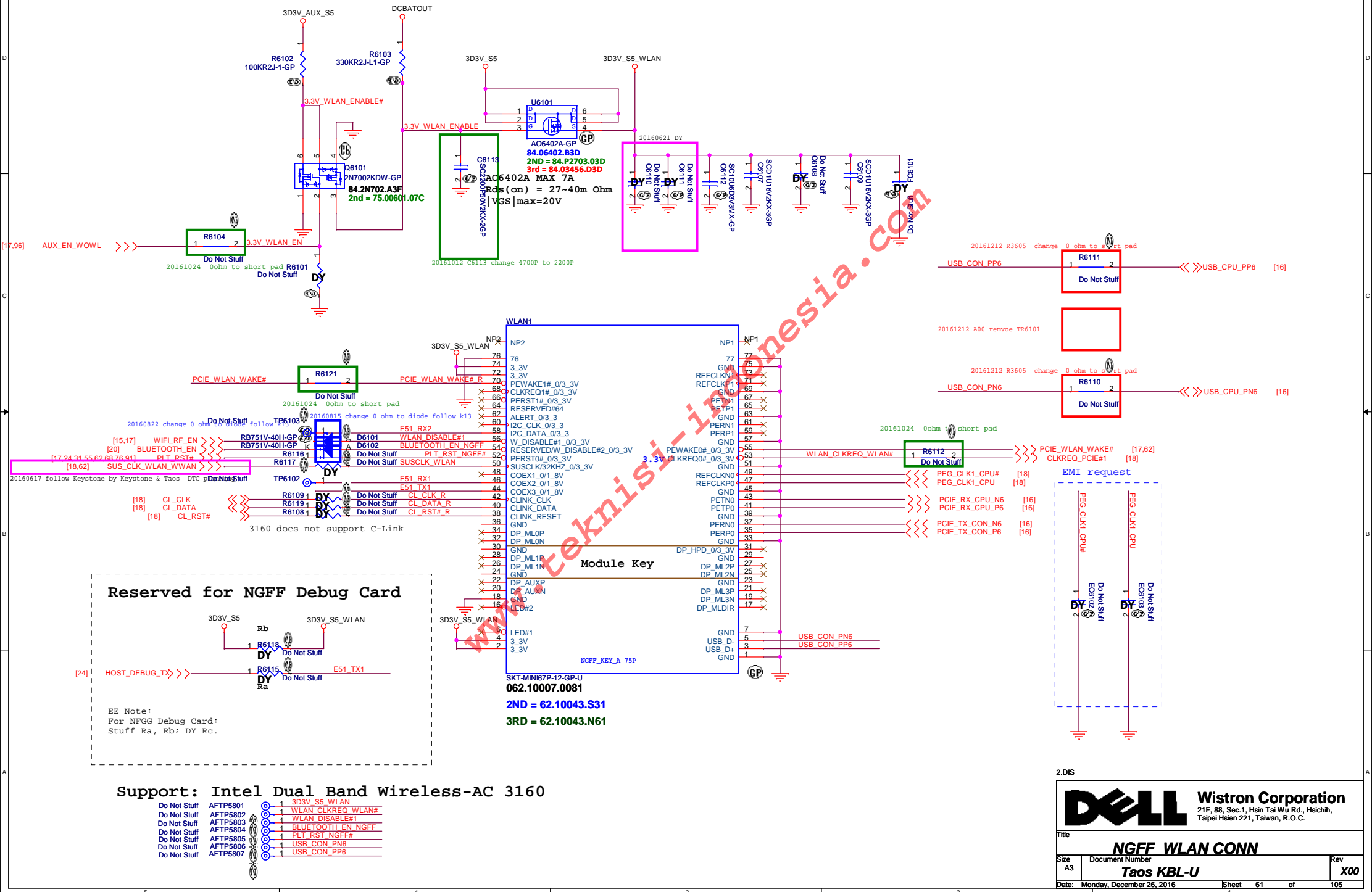
Taos KBL-U

Rev	Y00
-----	-----

Date: Monday, December 26, 2016

Sheet 60 of 105

Main Func = WLAN



Support: Intel Dual Band Wireless-AC 3160

Do Not Stuff	AFTP5801	3.3V_S5_WLAN
Do Not Stuff	AFTP5802	WLAN_CLKREQ_WLAN#
Do Not Stuff	AFTP5803	WLAN_DISABLE#
Do Not Stuff	AFTP5804	BLUETOOTH_EN NGFF
Do Not Stuff	AFTP5805	PLT_RST NGFF#
Do Not Stuff	AFTP5806	USB_CON_PN6
Do Not Stuff	AFTP5807	USB_CON_PP6

2.DIS

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

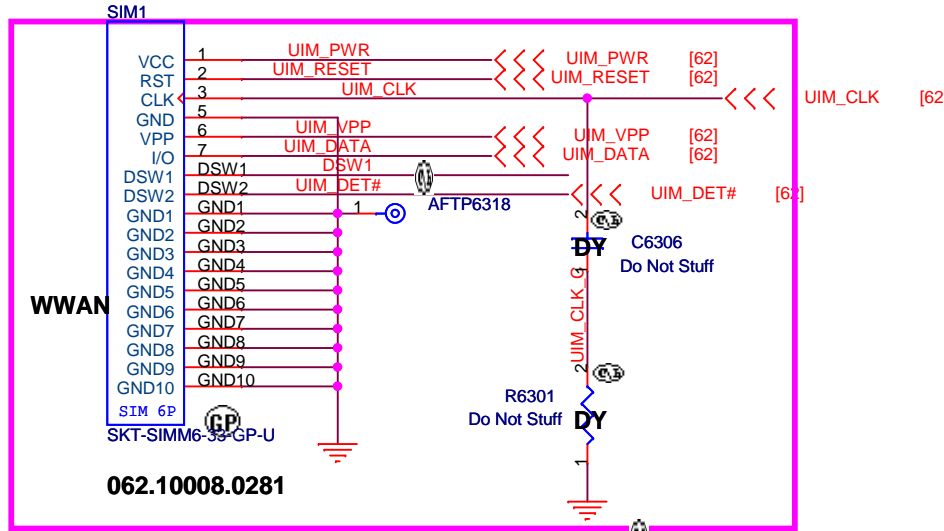
Title: **NGFF WLAN CONN**

Size: A3	Document Number: Taos KBL-U	Rev: X00
Date: Monday, December 26, 2016	Sheet: 61	of 105

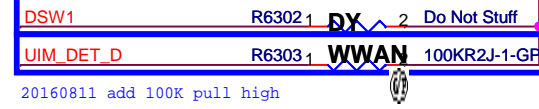
$$NGFF(WWAN/SSD)$$

SSID =WIRELESS

20160527 modify connector

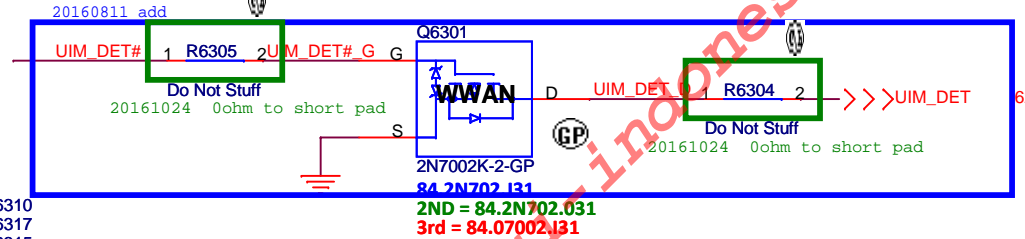
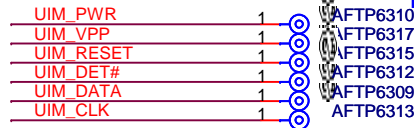


20160811 DY

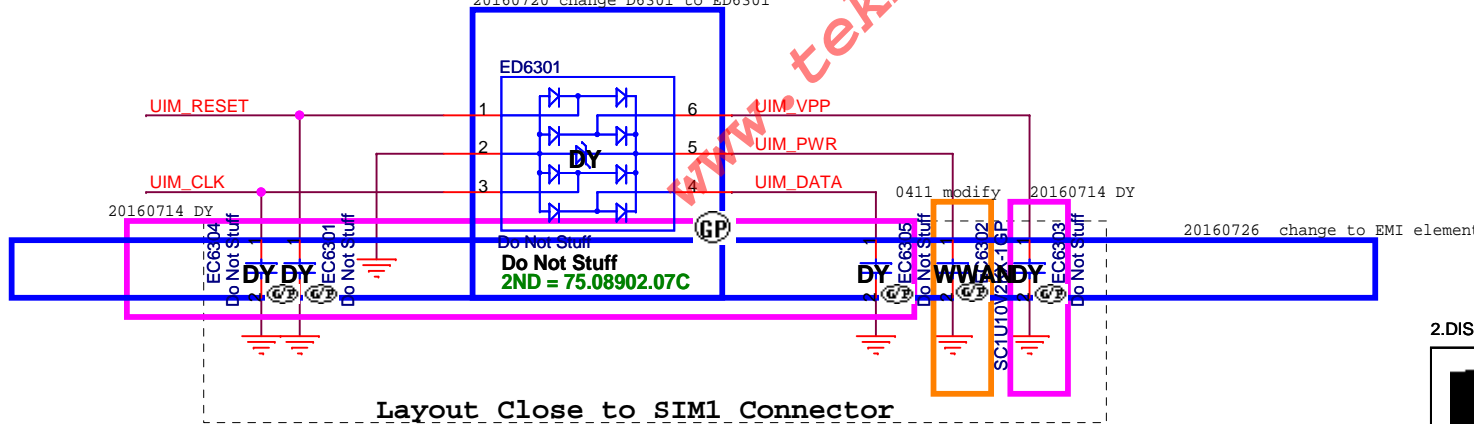


3D3V_S5_WWAN

PIN	62.10034.561 Micro SIM PinDefine
C1	VCC
C2	RST
C3	CLK
C4	Reserve
C5	GND
C6	VPP
C7	I/O
SW	SIM Card Detect
8	PTH GND
9	PTH GND
10	PTH GND
11	PTH GND



20160720 change D6301 to ED6301



Layout Close to SIM1 Connector

2.DIS

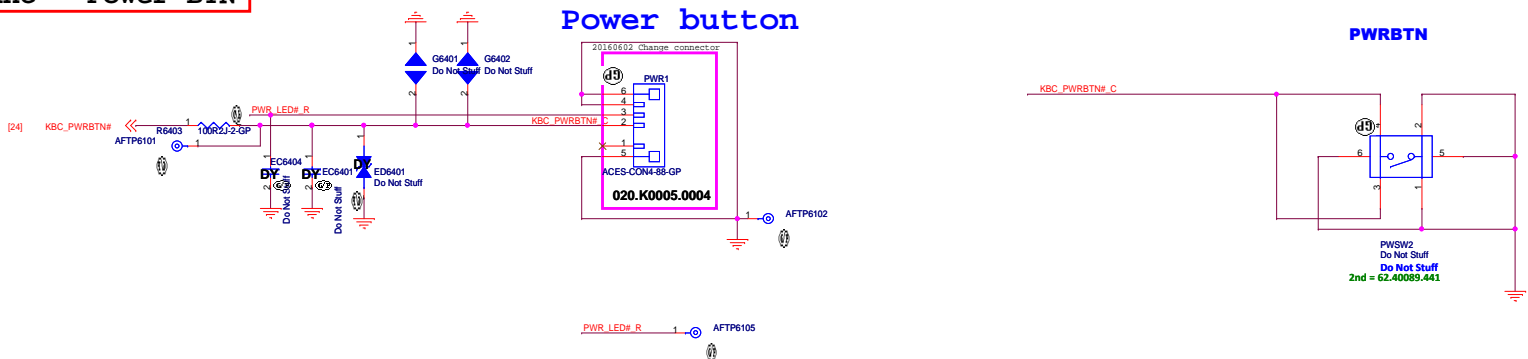
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)

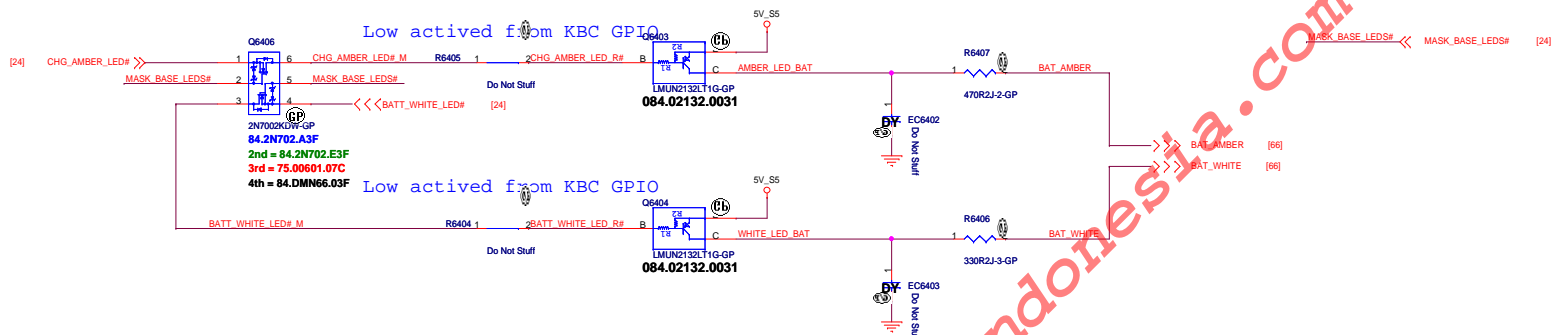
Size: A4 Document Number: Taos KBL-U Rev: X00

Date: Monday, December 26, 2016 Sheet: 63 of 105

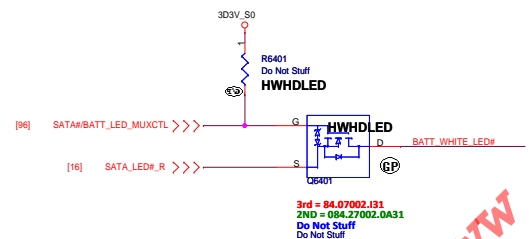
Main Func = Power BTN



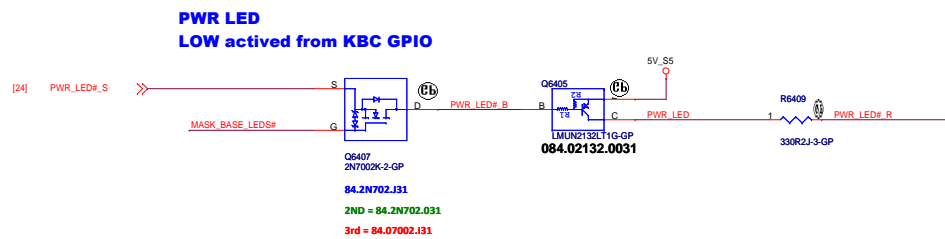
Main Func = Battery LED



Main Func = HDD LED



Main Func = PWR LED

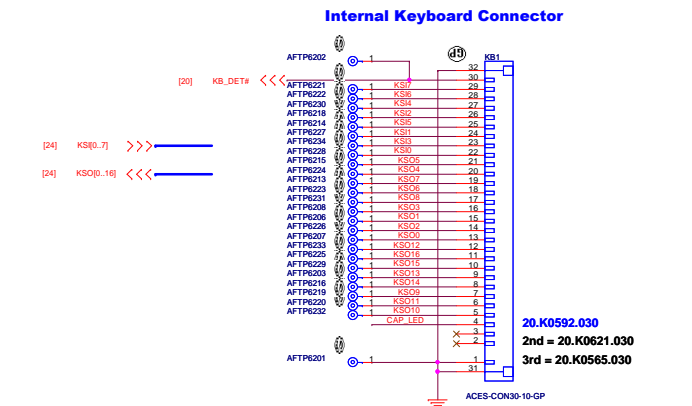


For EMI Reserved

PWR_LED

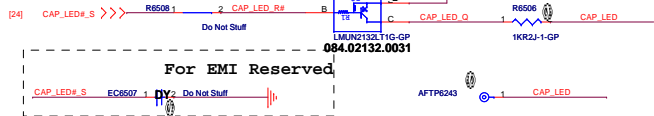
EC6406

Do Not Stuff

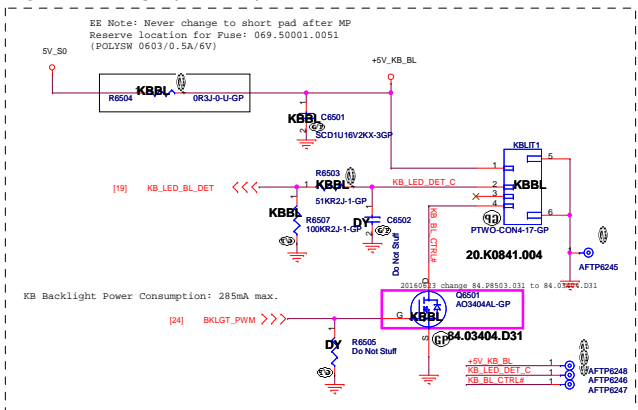


CAP LED Control

LOW acted from KBC GPIO



Keyboard Backlight (Reserved)

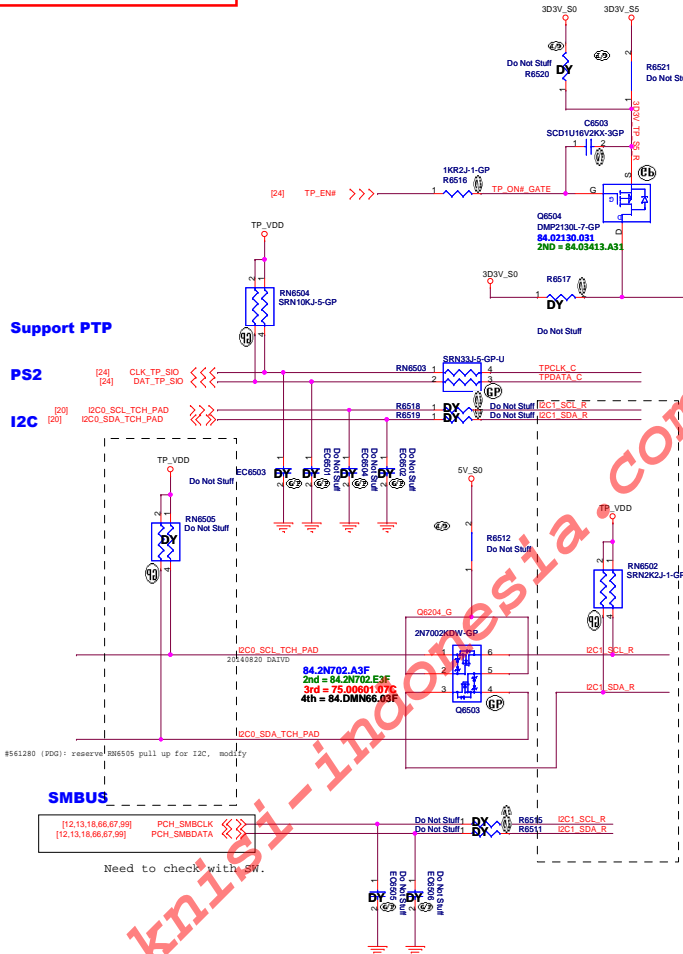


Support PTP

PS2

I2C

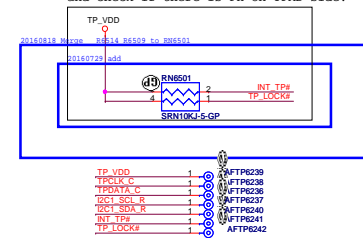
SMBUS



Precision Touch Pad Connector

Pin number	Pin name
8	VDD
7	DAT (I2C)
6	CLK (I2C)
5	GND
4	ATTN
3	GPIO
2	DAT (PS2)
1	CLK (PS2)

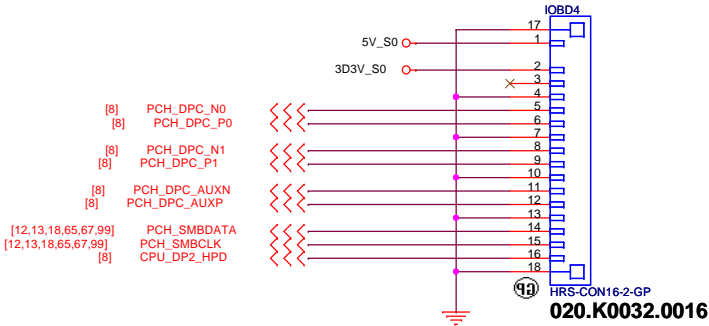
Need to check if it is Active High or Active Low and check if there is PH on TPAD side.



2.0IS

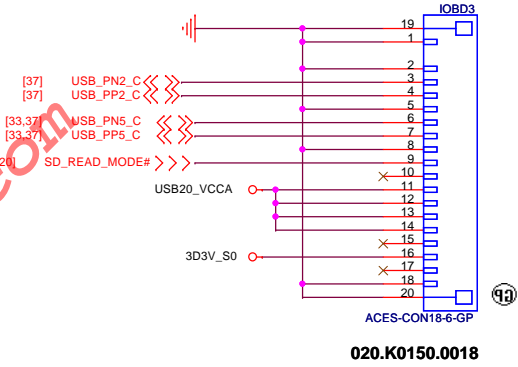
Main Func = IO Connector

VGA Connector



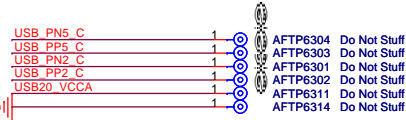
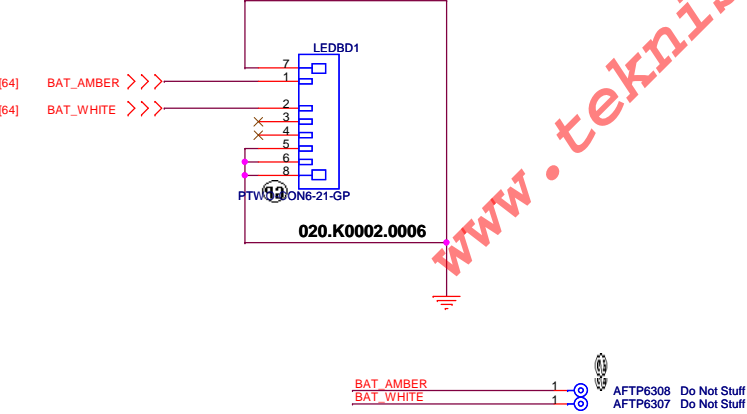
I/O Board Connector

USB3 (USB2.0)
Cardreader (USB2.0)

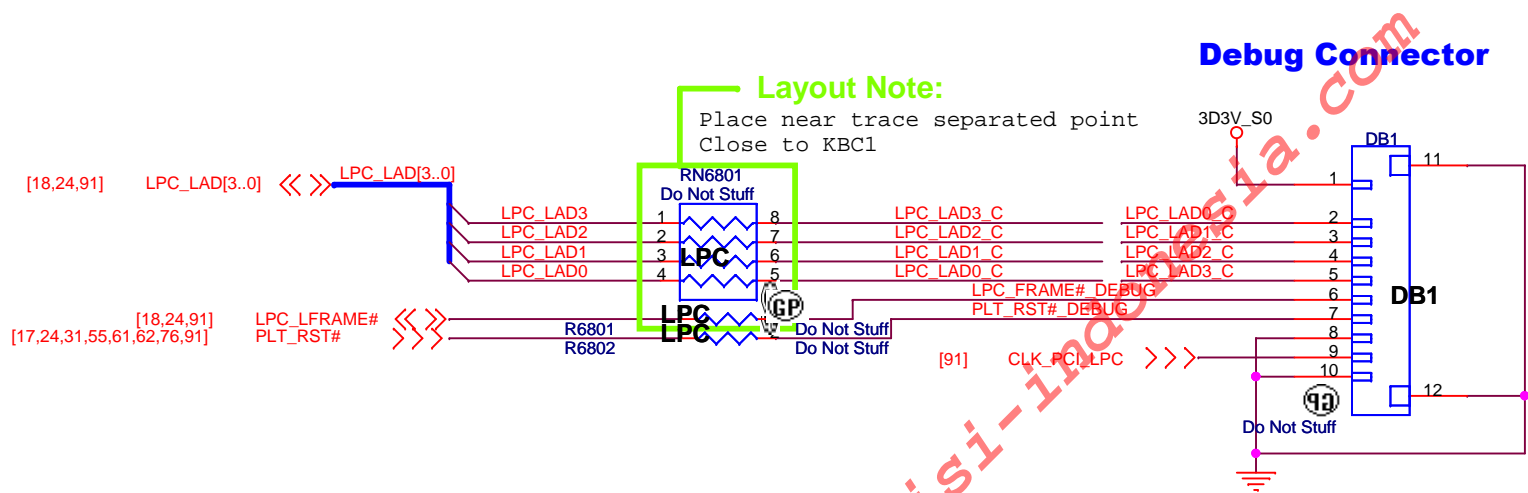


Pitch: 1mm
Power: 5 pins
GND: 5 pins

LED Connector



Main Func = Debug




Debug Connector

Do Not Stuff

20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.


2.DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Dubug connector			
Size A4	Document Number Taos KBL-U		Rev X00
Date: Monday, December 26, 2016		Sheet 68	of 105

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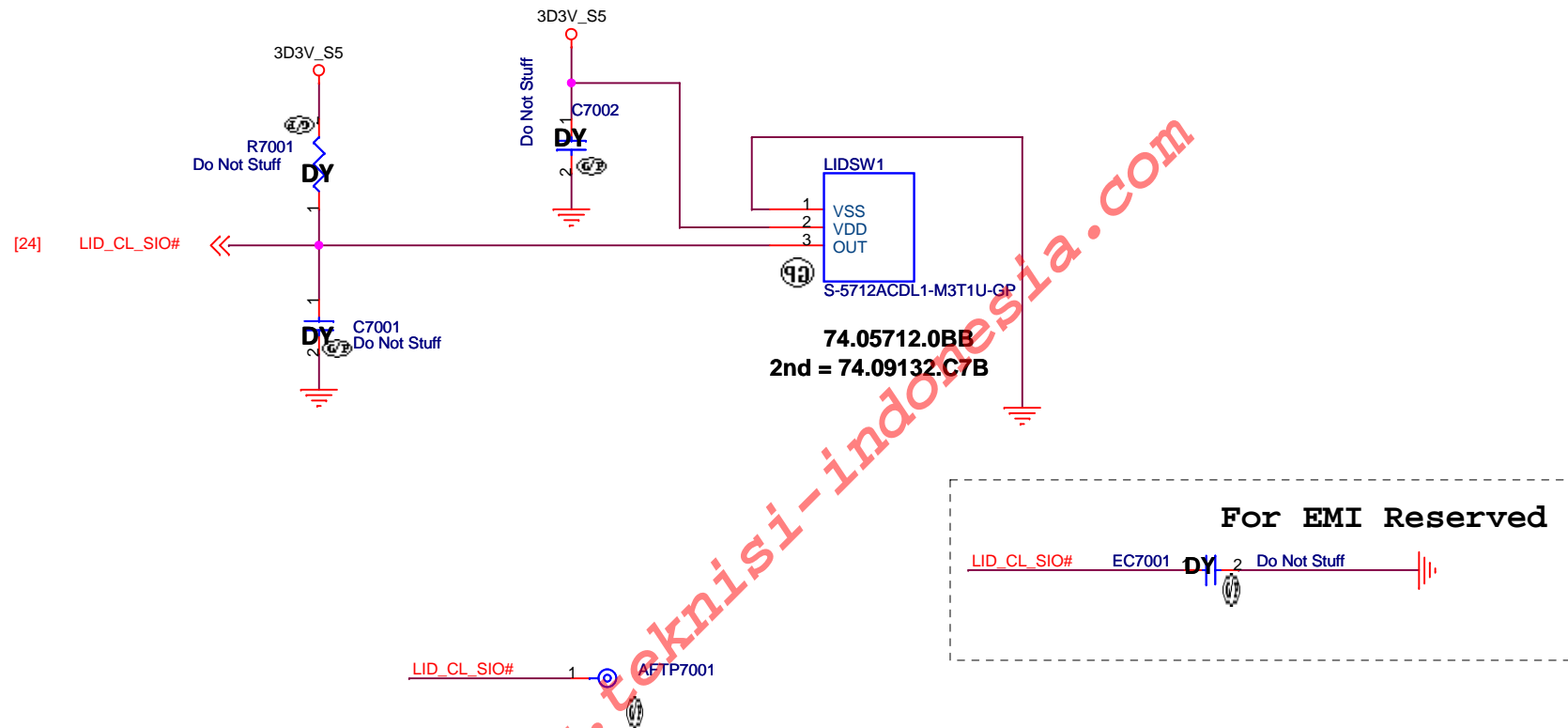
(Blanking)

2.DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A4	Document Number Taos KBL-U		Rev X00
Date: Monday, December 26, 2016		Sheet 69	of 105

Main Func = Hall Sensor

LID sensoe




2.DIS

DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number Taos KBL-U		Rev X00
Date: Monday, December 26, 2016		Sheet 70 of 105	

(Blanking)

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Title

Size
A4

Document Number
Taos KBL-U

Rev
X00

Date: Monday, December 26, 2016Sheet 71 of 105

(Blanking)

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Title			
USB3.0 PORT			
Size	Document Number		Rev
A4	Taos KBL-U		X00
Date:	Monday, December 26, 2016		Sheet 72 of 105

Main Func = dGPU


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2.DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <i>Thunderbolt (3/5)(Reserved)</i>			
Size A4	Document Number Taos KBL-U		Rev X00
Date: Monday, December 26, 2016		Sheet 73 of	105


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2.DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title Thunderbolt (4/5)(Reserved)		
Size A4	Document Number Taos KBL-U	Rev X00
Date: Monday, December 26, 2016		Sheet 74 of 105

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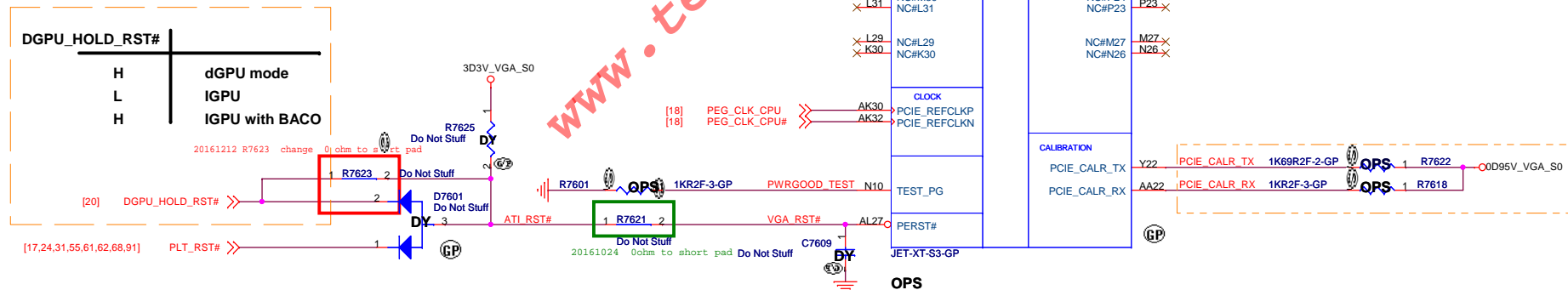
2.DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <i>Thunderbolt (5/5)(Reserved)</i>		
Size A4	Document Number Taos KBL-U	Rev X00
Date: Monday, December 26, 2016		Sheet 75 of 105

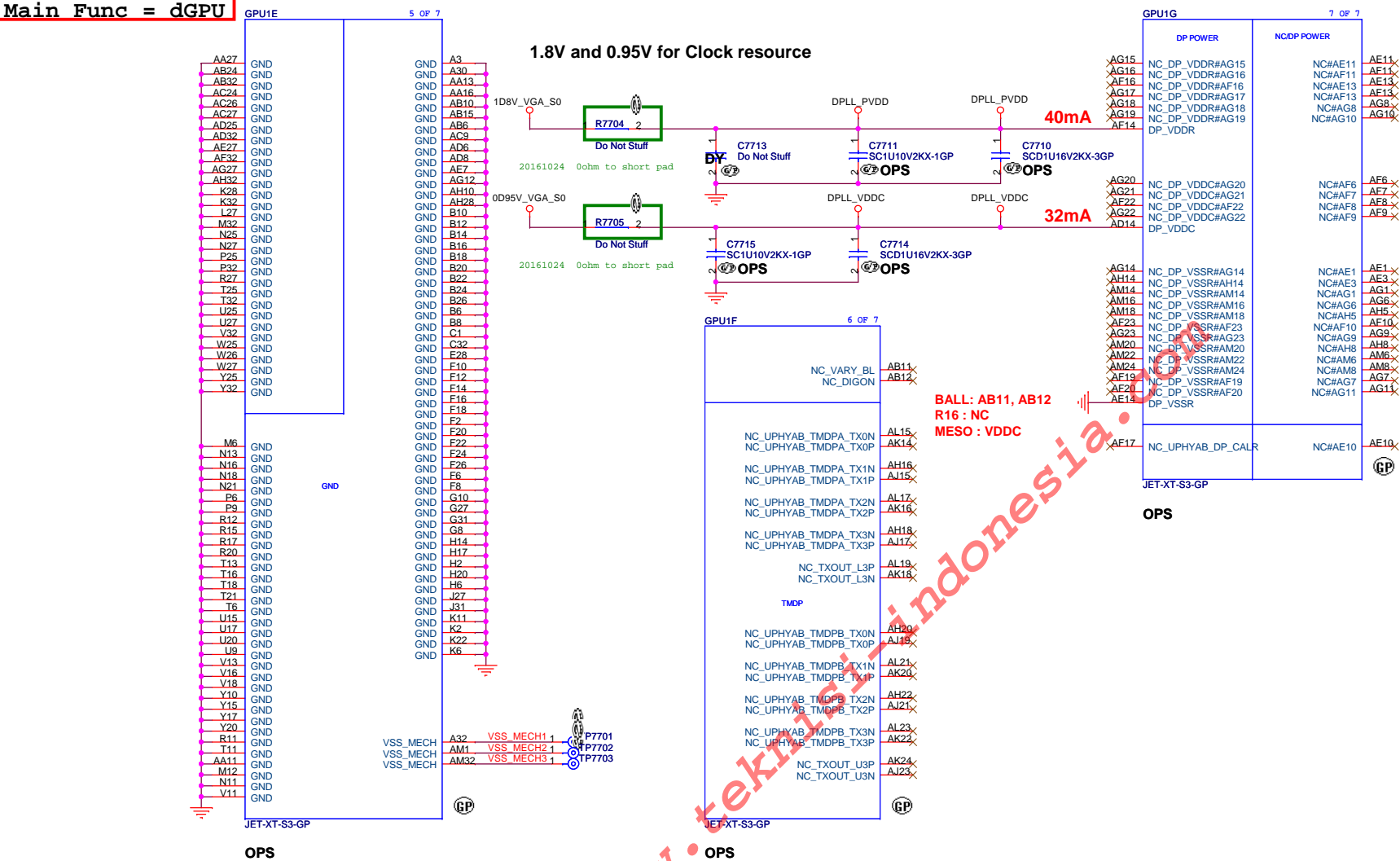
GFX & GPP, 85Ω
GFX & GPP CLK, 85Ω
GPU1A

Table 3-5 PCI Express® Bus Interface

Pin Name	I/O	Description
PERSTb	I	Fundamental reset. 3.3-V tolerant pad. This signal must be asserted during any fundamental reset event, such as power on, warm boot, reset button pressed, CTL-ALT-DEL, Windows restart, or wake from D3.
PCIE_REFCLKP/N	I	PCI Express PLL differential reference clock (+/-). 100-MHz (\pm 300 ppm) input frequency; 0-V to 0.7-V single-ended swing.
PCIE_TX[7:0]P/N	O	PCI Express transmitter output data channel TX[7:0] (+/-). Differential serial data transmitted up to a 8.0-GT/s bit rate.
PCIE_RX[7:0]P/N	I	PCI Express receiver input data channel RX[7:0] (+/-). Differential serial data received up to a 8.0-GT/s bit rate.
PCIE_CALR_RX	I	Connect to PCIE_VDDC through a 1-k Ω (1% tolerance) resistor.
PCIE_CALR_TX	I	Connect to PCIE_VDDC through a 1.69-k Ω (1% tolerance) resistor.
CLKREQb	O	Reserved, do not connect on the PCB.

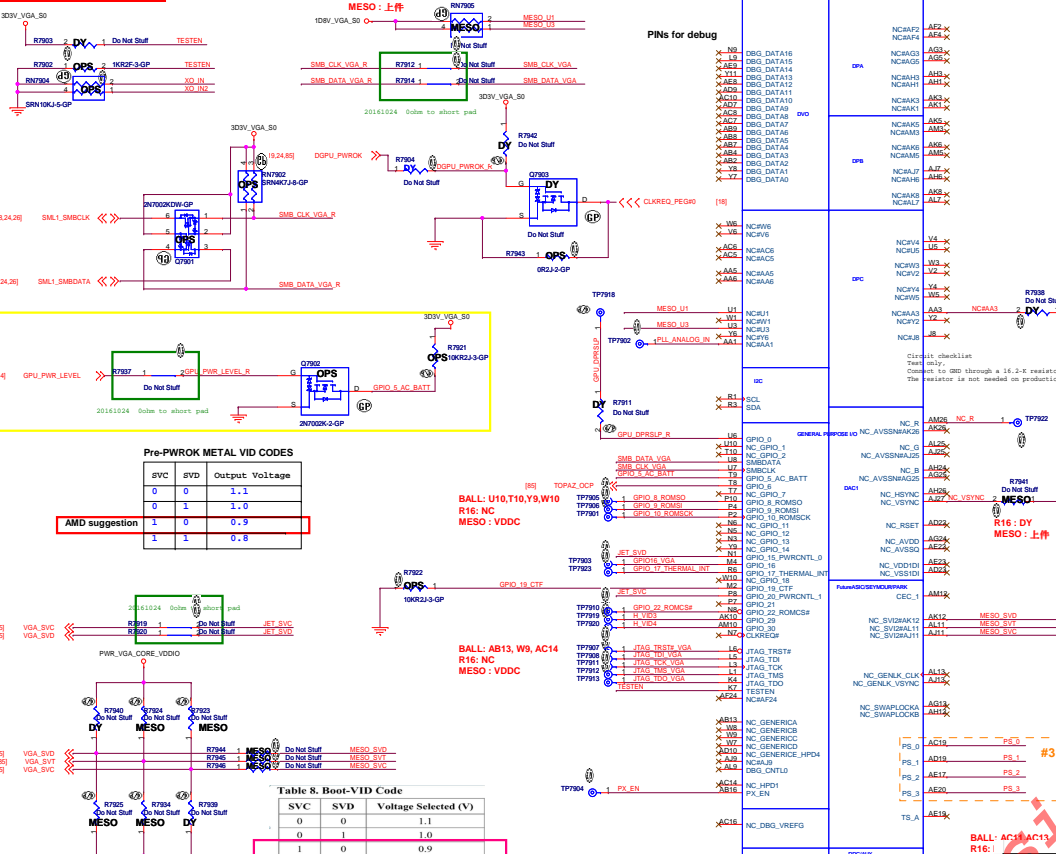


Main Func = dGPU

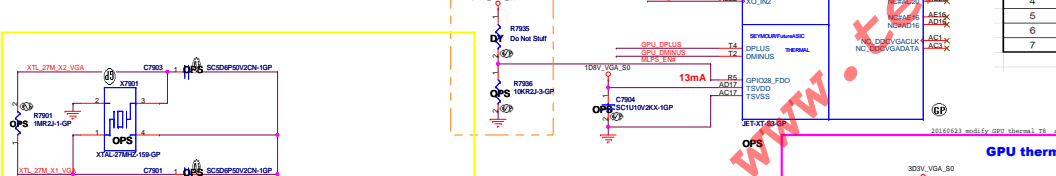


X00

Main Func = dGPU

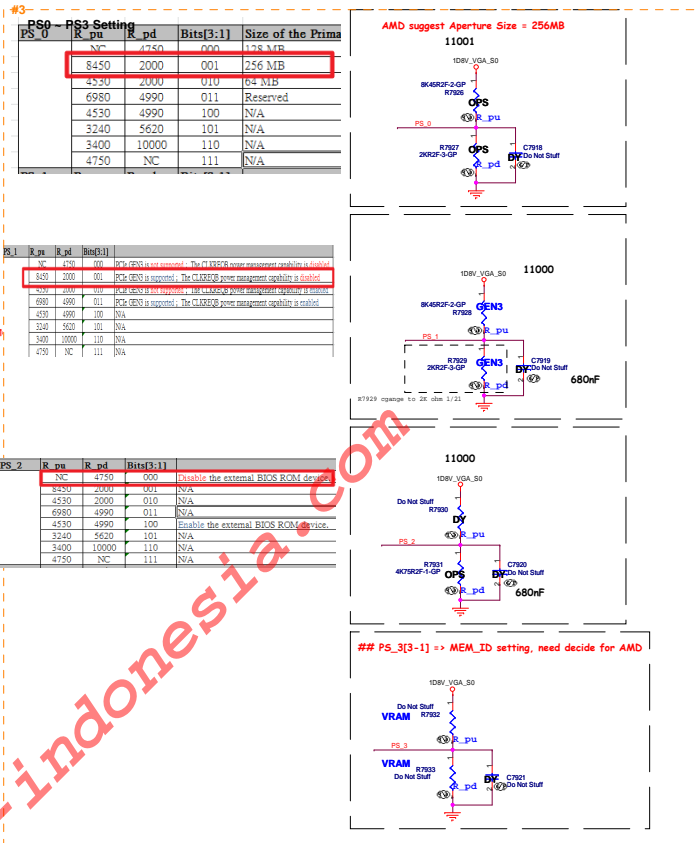


	SVID	PWR Sequencing
R16	R7919 R7920	PR8611 PC8607 / PR8612 PC8611



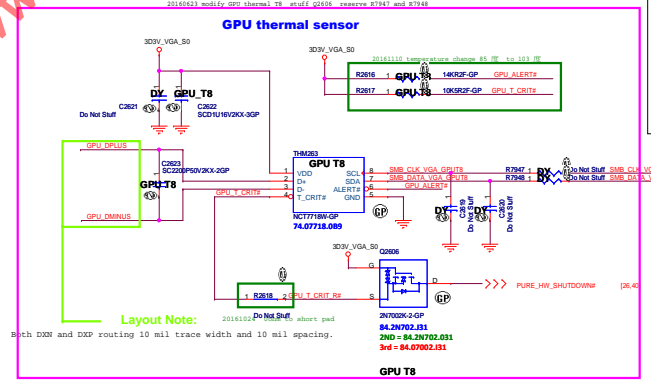
Note :
C7501 and C7503 values determine CL value of the oscillation circuit.
If Negative Resistance is too low, that may cause crystal resonator stop oscillation or not easy to oscillate.
If Drive Level is too high, that may cause crystal resonator abnormal oscillation or damaged the main body of quartz.

TEMPERATURE(°C)		T_CRIT#				
		2K Ω	7.5K Ω	10.5K Ω	14K Ω	18.7K Ω
ALERT#	2K Ω	77	87	97	107	117
	7.5K Ω	79	89	99	109	119
	10.5K Ω	81	91	101	111	121
	14K Ω	83	93	103	113	123
	18.7K Ω	85	95	105	115	125



MLPS Memory ID setting:									
BOARD_CONFIG[2:0]									
ID	ID_00	Memory Type	Configuration	Row x Col x Bank bits	Channel Size	Vendor PIN	SMT quantity	R_00s	R_04s
0	000	Samsung - DDR3L	256M x 16		2GB	K4W4G1648E-BC1A	4 pcs	30C	4750
1	001	Micron - DDR3L	256M x 16		2GB	MT41J256M16LY-0910-N	4 pcs	8450	2000
2	010	SK hynix - DDR3L	256M x 16		2GB	H5TC4J663EPR-N0C	4 pcs	4530	2000
3	011								
4	100								
5	101								
6	110								
7	111								

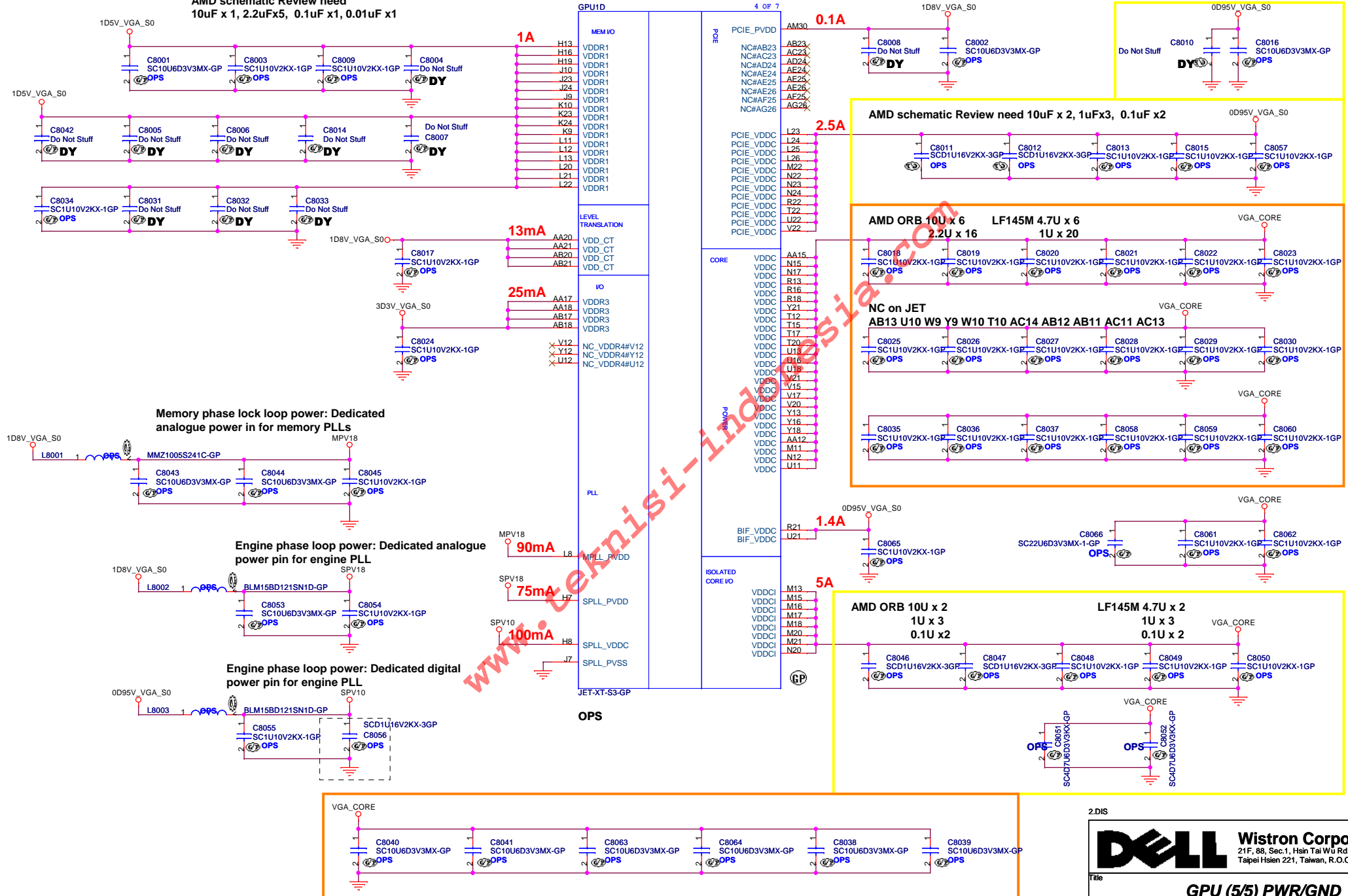
Resistor	Capacitor
4.75Kohm: PN/64.47515.6DL	680nF: PN/78.68421.5BL
8.45Kohm: PN/64.84515.6DL	82nF: PN/78.82321.2FL
2Kohm: PN/64.20015.6DL	10nF: PN/78.10324.10L
4.53Kohm: PN/64.45315.6DL	
6.98Kohm: PN/64.69815.6DL	
4.99Kohm: PN/64.49915.6DL	
3.24Kohm: PN/64.32415.6DL	
3.4Kohm: PN/64.34015.6DL	
5.62Kohm: PN/64.56215.6DL	
10Kohm: PN/64.10025.6DL	



Main Func = dGPU

20160701 decap follow decap plan file

AMD schematic Review need
10uF x 1, 2.2uFx5, 0.1uF x1, 0.01uF x1



2.DIS



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

	Title
--	-------

GPU (5/5) PWR/GND

Size

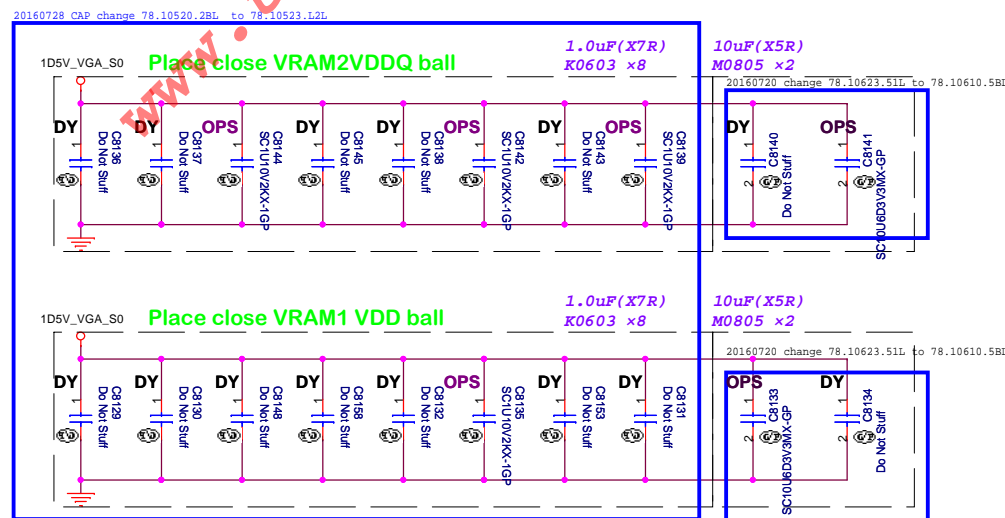
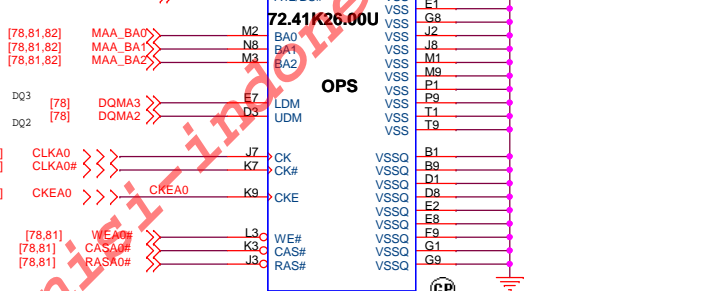
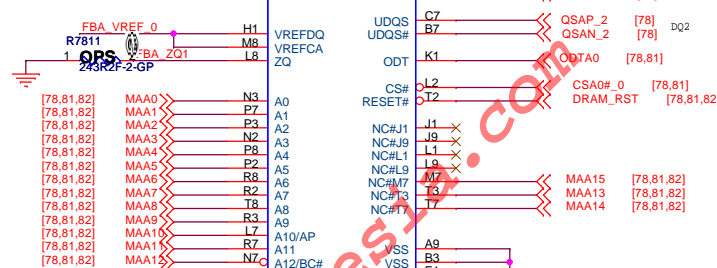
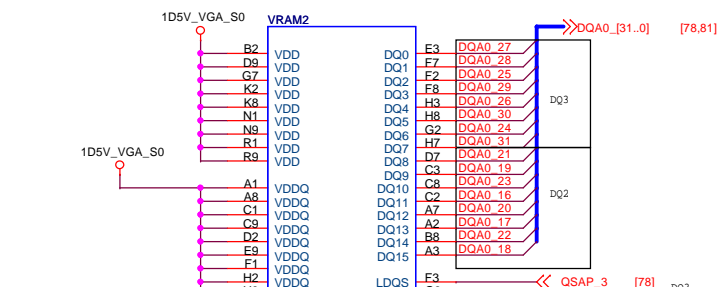
Document No.

Taos KBL-U

Date: Monday, December 26, 2016

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20160701 decan follow decan plan file

[illegible]

1D5V_VGA_S0

0.1uF(X7R)
K0402 x4

Do Not Suffer

C8154 DY

Do Not Suffer

C8156 DY

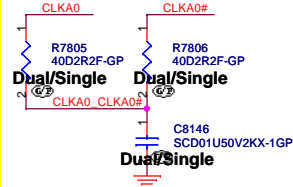
SC01U6V2X00-3GP

C8155 OPS

Do Not Suffer

C8157 DY

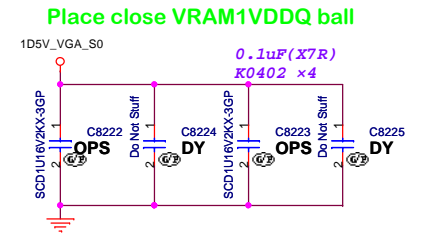
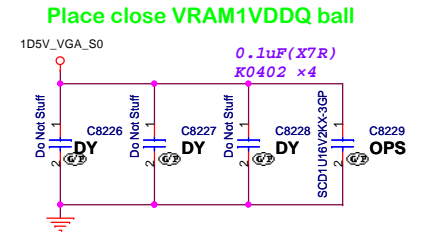
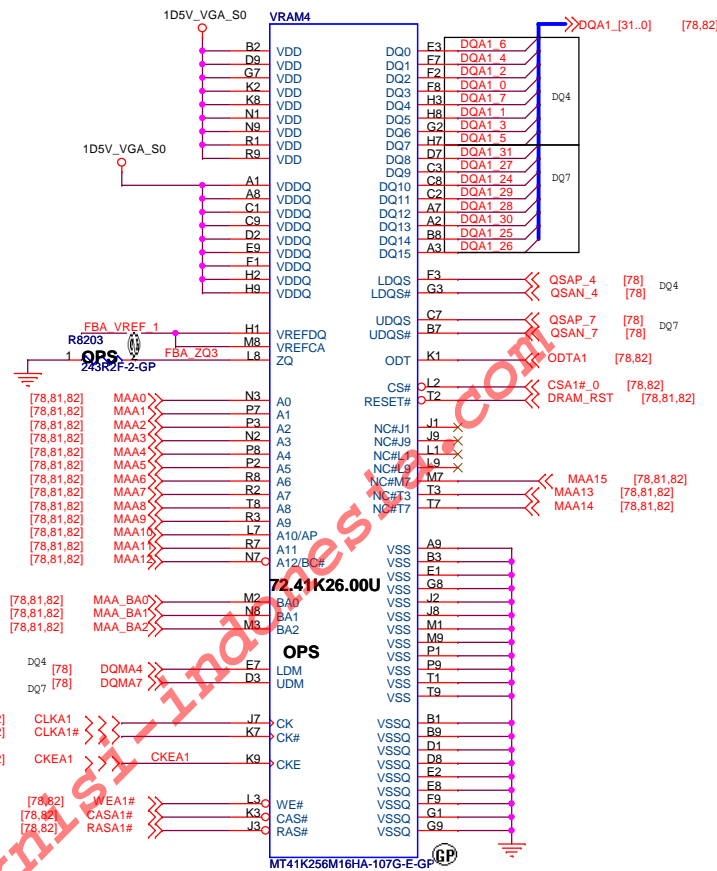
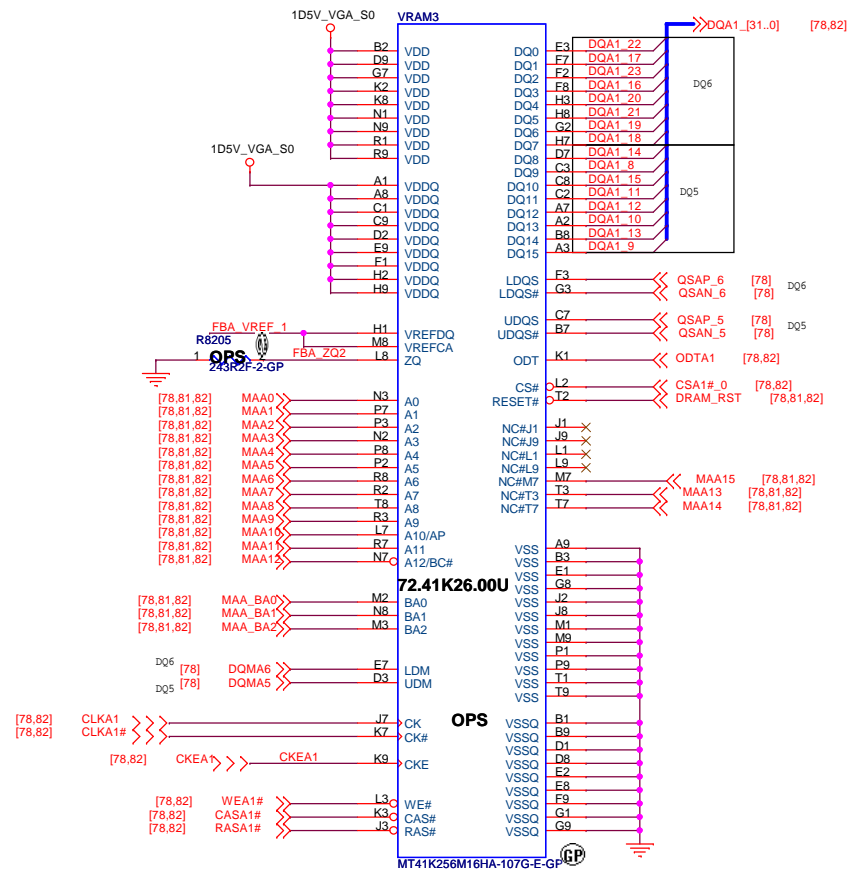
Single Rank, 40.2 Ohm = 64.40R25.6DL
Dual Rank, 80.6 Ohm = 64.80R65.6DL



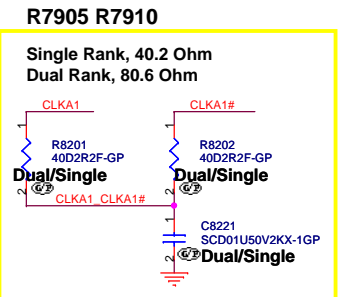
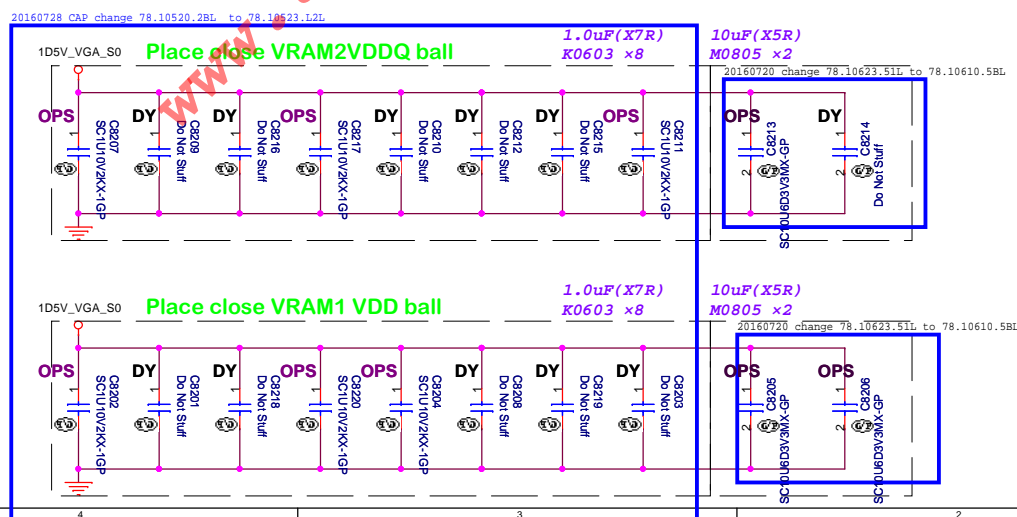
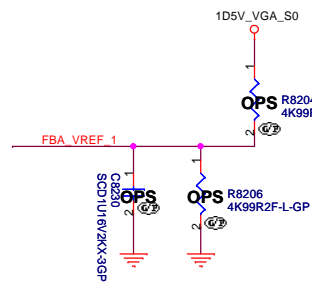
2.DIS



Title			
VRAM1,2 (1/4)			
Size A3	Document Number		Rev
	Tao KBL-U		X00
Date:	Monday, December 26, 2016	Sheet 81 of	105

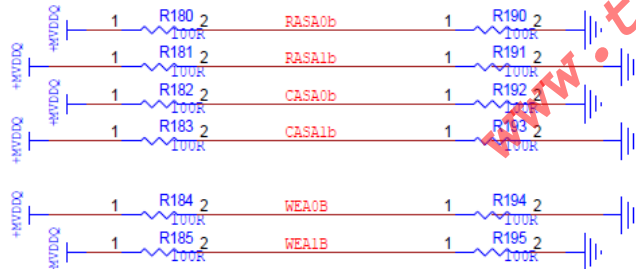
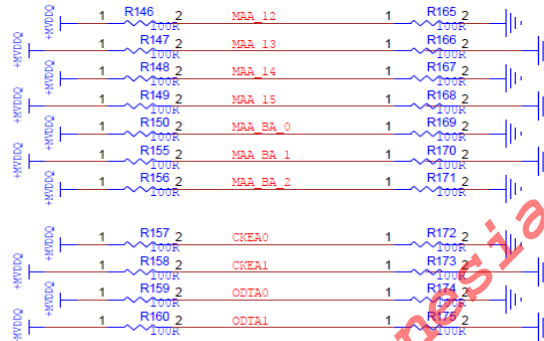
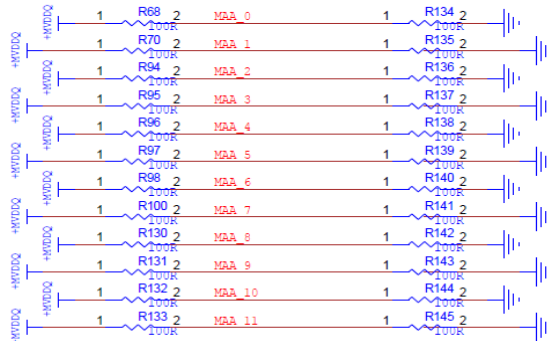


Frame Buffer Partition A-Lower Half



Note : Dual Rank need add

For DUAL RANK configuration,
termination might be required based on simulation results
the actual termination value should be OPTIMIZED by the simulation



2.DIS




Title			(Reserved) VRAM5,6 (3/4)
Size	Document Number	Rev	X00
A3	Taos KBL-U		
Date: Monday, December 26, 2016			Sheet 83 of 105

Main Func = dGPU

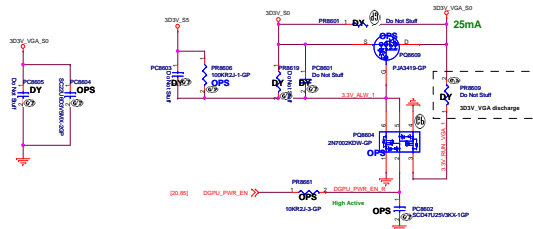
Data Bits 63:32 RANK 1

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2.DIS

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved) VRAM7,8 (4/4)			
Size A4	Document Number Taos KBL-U		Rev X00
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3D3V_S0 to 3D3V_VGA_S0 Transfer



GPU PWR Sequencing

3D3V_VGAS0

=> 0D95V_VGA_S0/1D8V_VGA_S0

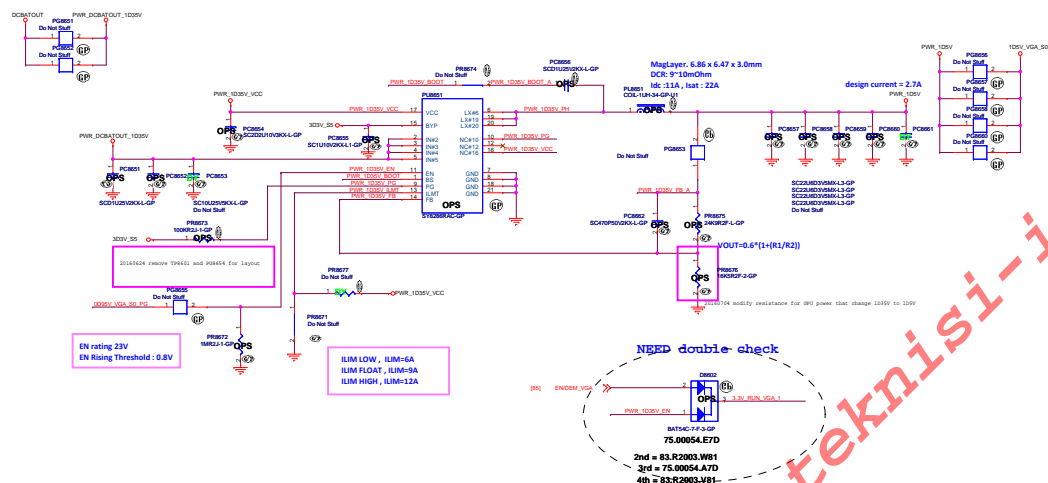
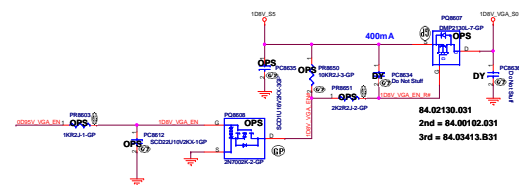
=> 1D35V_VGA_S0

=> VGA_CORE

All the ASIC supplies must reach their respective nominal voltages within **20ms** of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50mV/us.

It is recommended that the 3.3V rail ramp up first.

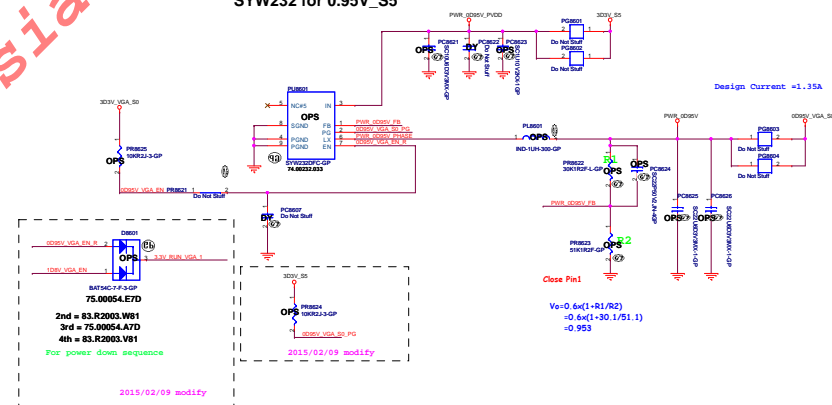
It is recommended that the 0.95V rail reach at least 90% of its normal value no later than 2ms from the start of VDDC ramping up.



~~NEED double check~~

2nd = 83.R2003.W81
3rd = 75.00054.A7D
4th = 83.R2003.V81

SYW232 for 0.95V S5



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Reserved			
Size A4	Document Number Taos KBL-U		Rev X00
Date: Monday, December 26, 2016		Sheet 88 of	105

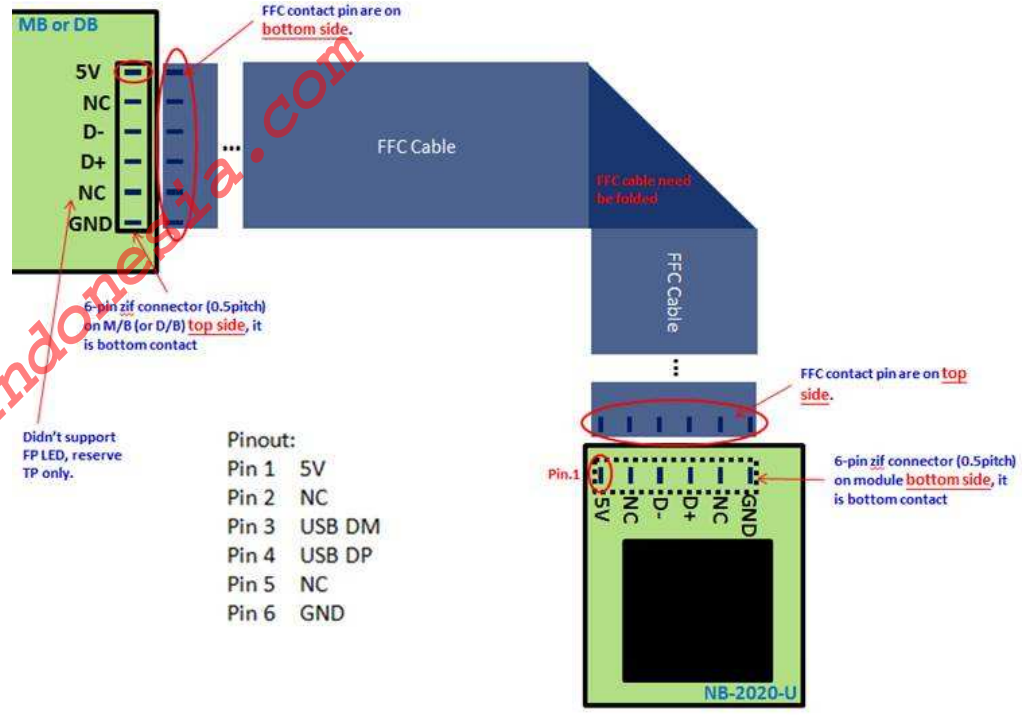
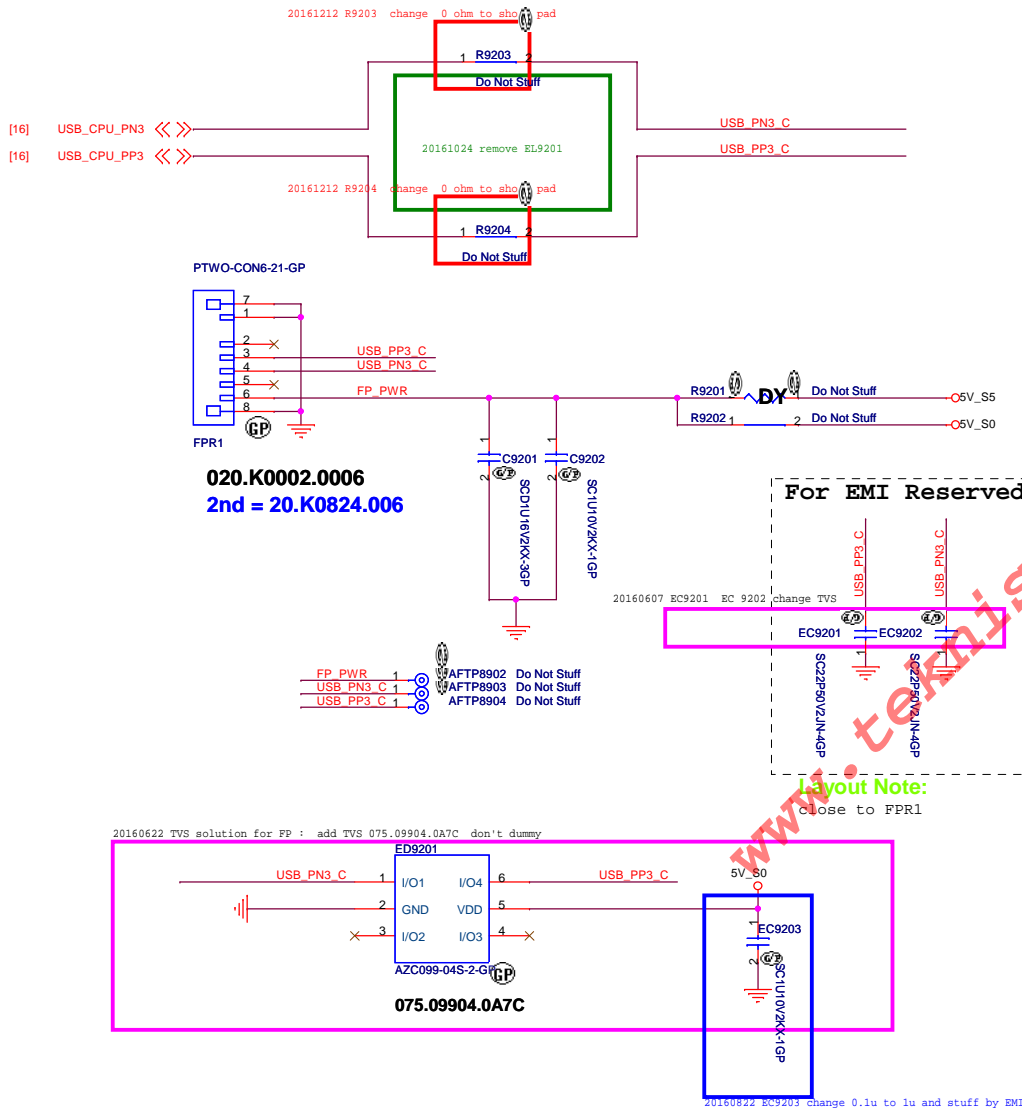
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SSID = Finger Print



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Size A4	Document Number Taos KBL-U		Rev X00
Date: Monday, December 26, 2016		Sheet 93 of	105

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2.DIS

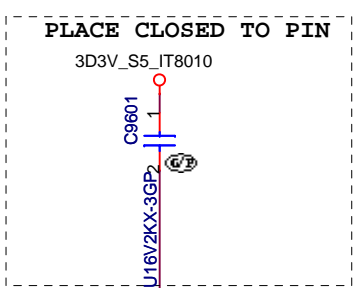
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Size A4	Document Number Taos KBL-U		Rev X00
Date: Monday, December 26, 2016		Sheet 94 of	105

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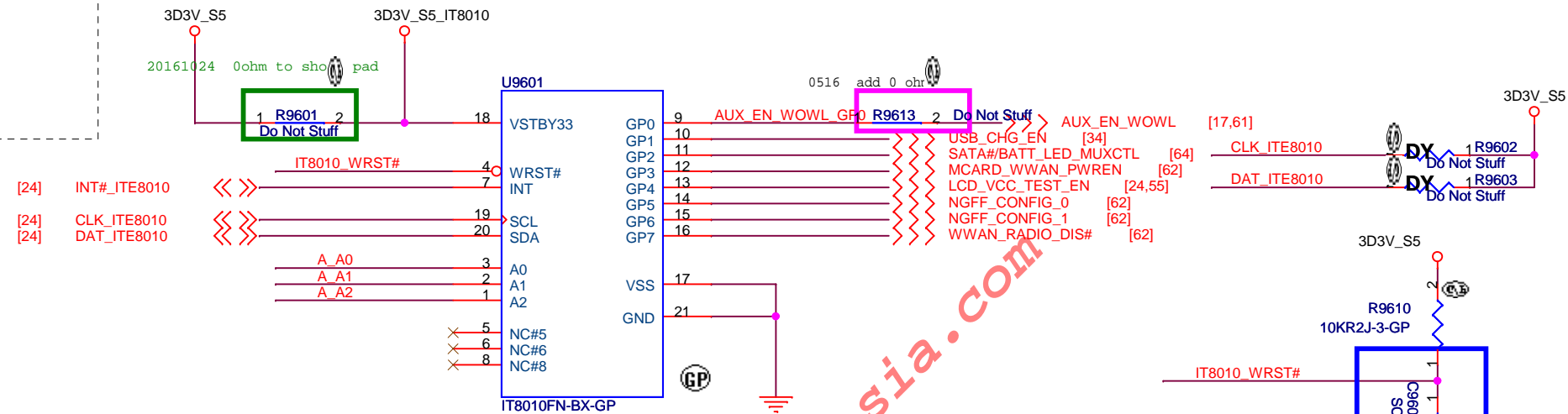
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Title (Reserved)			
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All I/O Signals are 3.3V CMOS Level



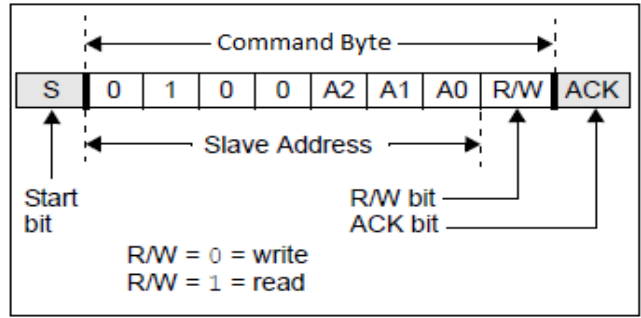
071.08010.0A03

IT8010/IT8011/IT8012 difference

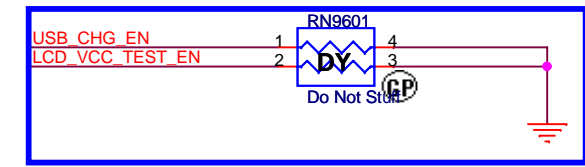
DEVICE	PIN8	PIN18
IT8010	NC	VSTBY33
IT8011	NC	VSTBY18
IT8012	VCOREI	VSTBY33

I2C SAD+Read/Write patterns

Command	SAD[7:4]	A[2]	A[1]	A[0]	R/W	SAD+R/W
Read	0100	0	0	0	1	01000001 (41h)
Write	0100	0	0	0	0	01000000 (40h)
Read	0100	0	0	1	1	01000011 (43h)
Write	0100	0	0	1	0	01000010 (42h)
Read	0100	1	1	1	1	01001111 (4Fh)
Write	0100	1	1	1	0	01001110 (4Eh)



20160720 follow vendor suggest change 0.1u to 1u, same with Keystone13



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Title: (Reserved)


Size: A4 Document Number: **Taos KBL-U** Rev: X00

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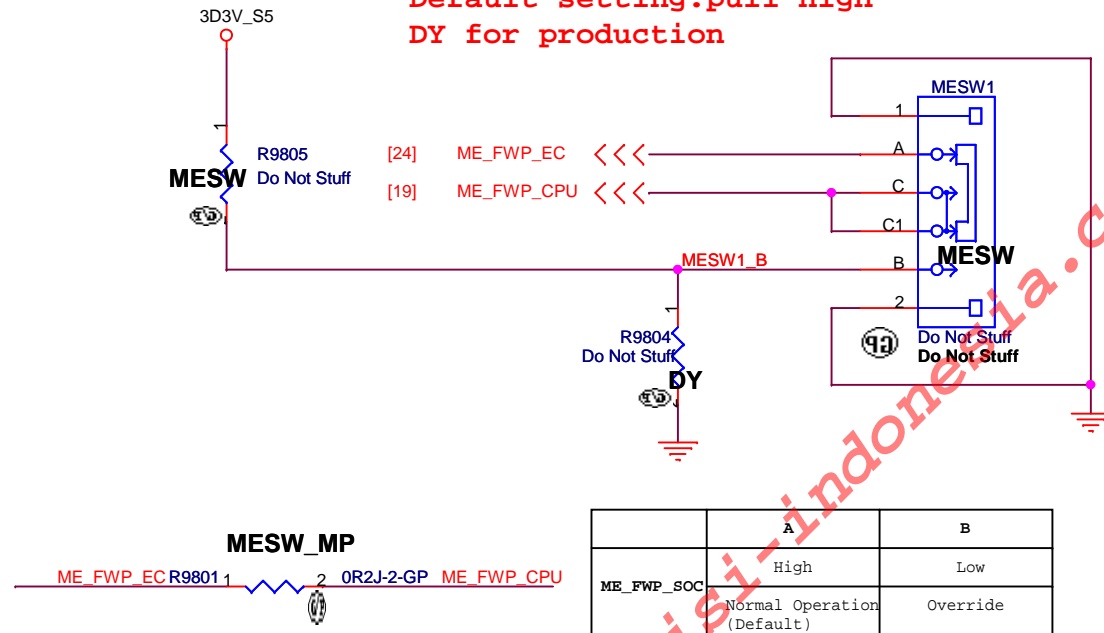
2.DIS

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Title LVDS Switch			
Size A4	Document Number Taos KBL-U		Rev X00
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20160707 follow Keystone add 3D3V_S5 pull high

Firmware SW

Default setting:pull high
DY for production



2.DIS



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Firmware SW

Size
A4

Document Number

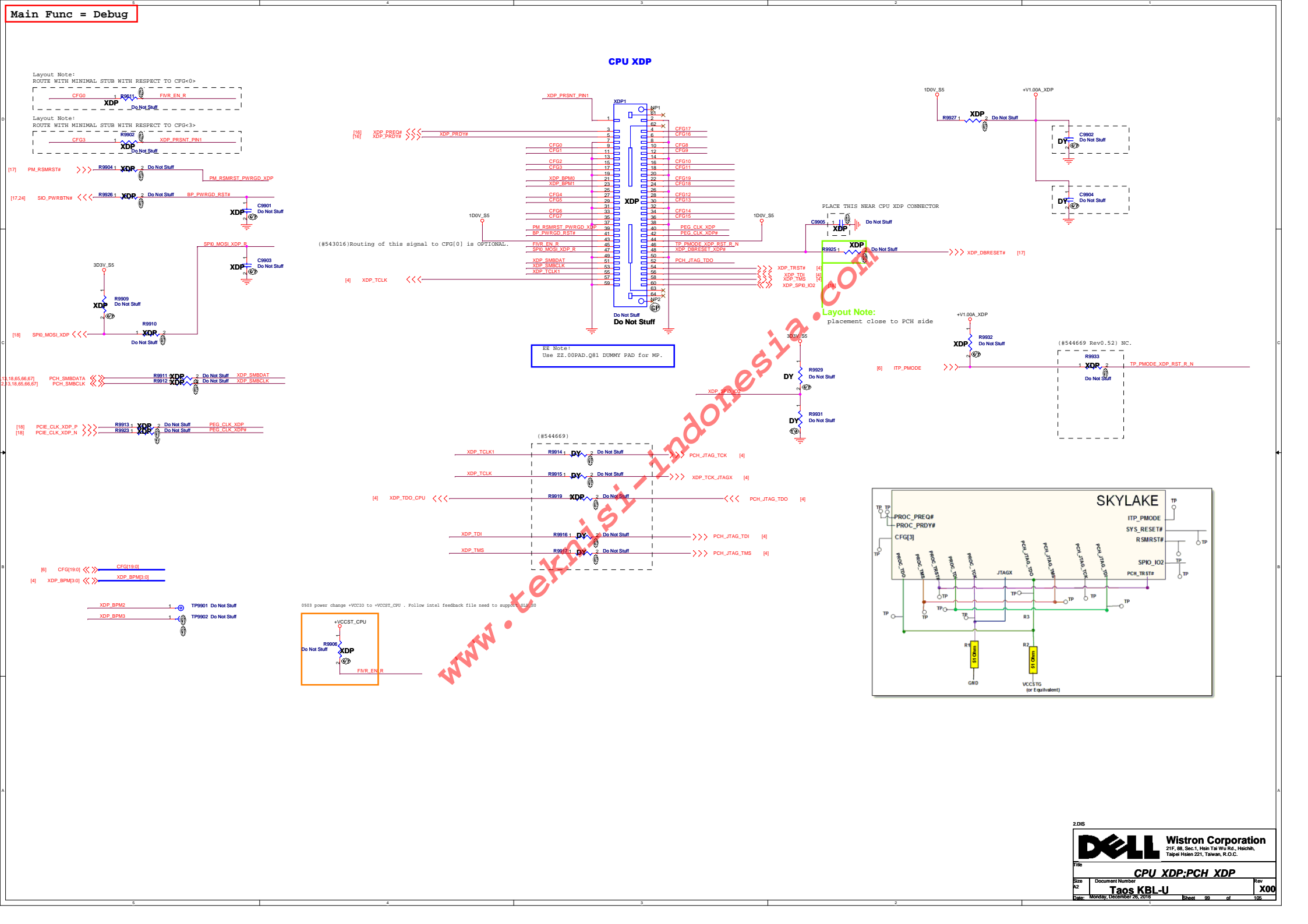
Taos KBL-U

Rev

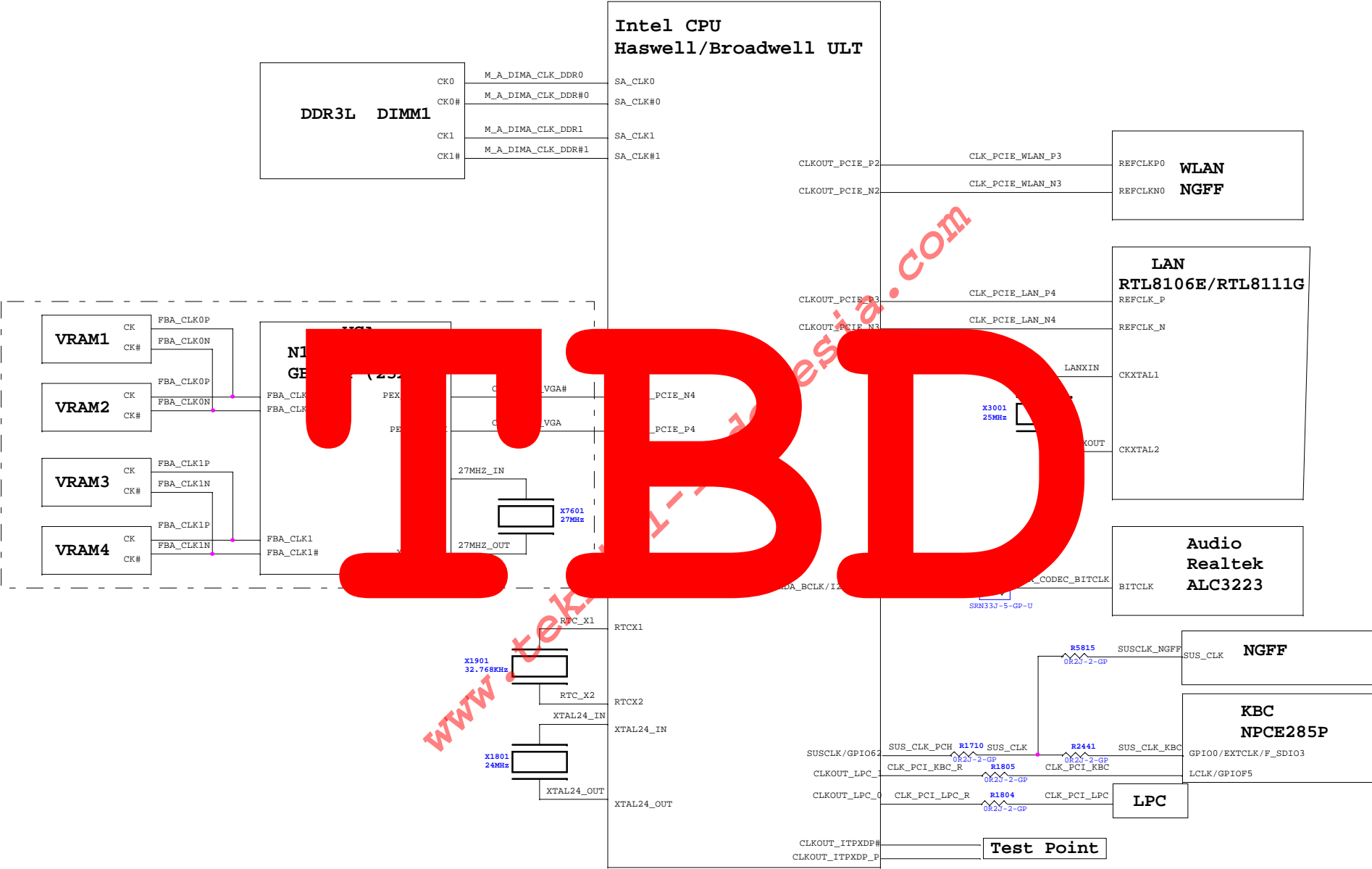
X00

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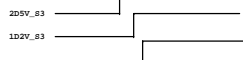


CLK Block Diagram



[illegible]

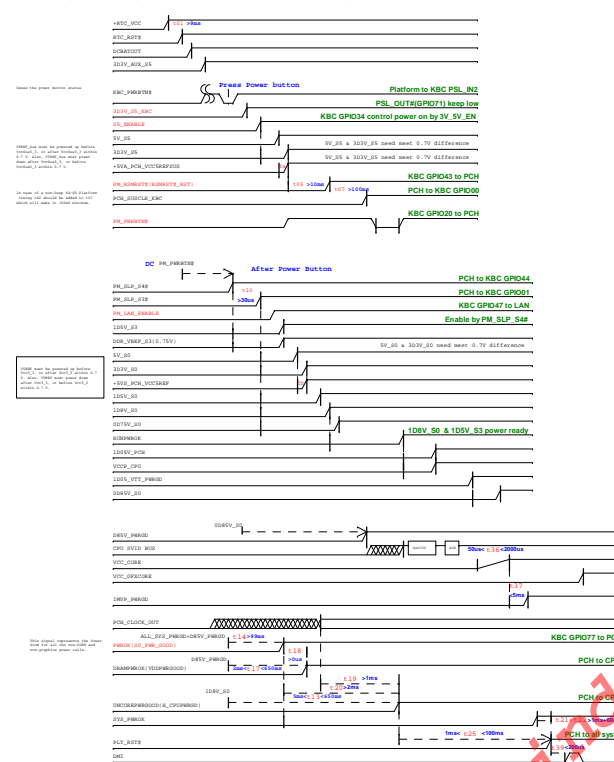
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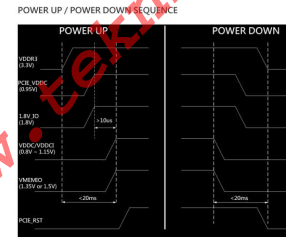
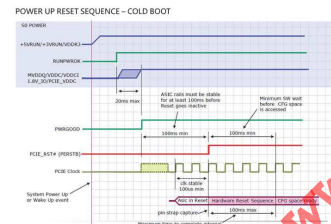
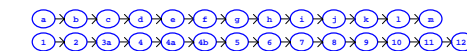
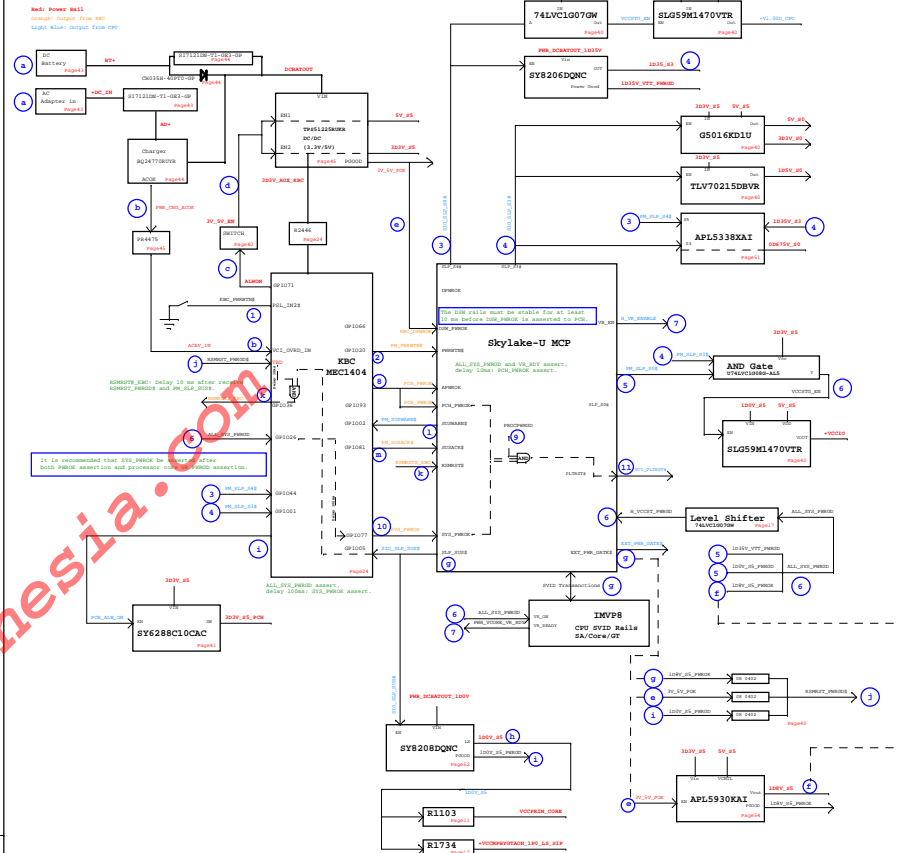


20ms
All the ASiC supplies must reach their respective nominal voltages withing of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum ramp-up time on all rails is 500µs.
It is recommended that the 3.3V rail ramp up first.
It is recommended that the 0.95V rail reach at least 90% of its normal value no later than 2ms from the start of VDDC ramping up.

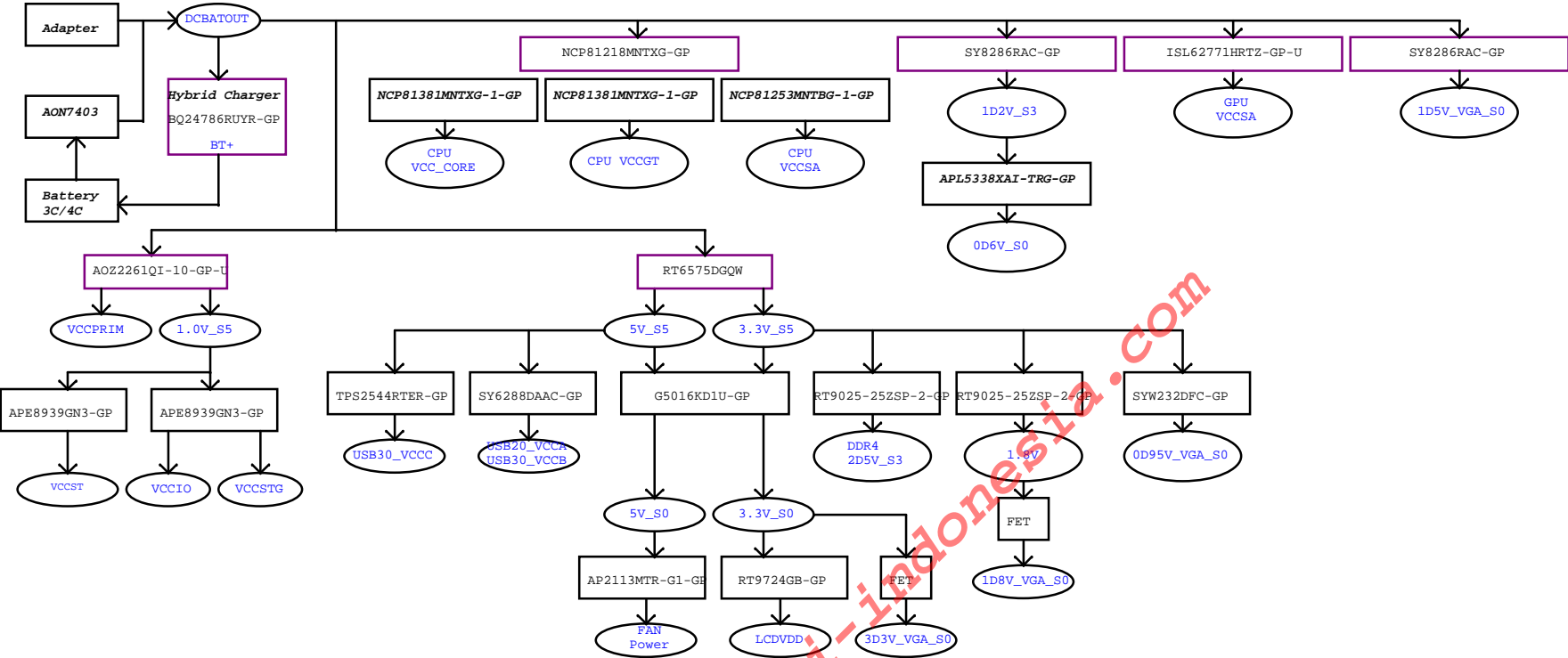


Red Words: Controlled by EC GPI:

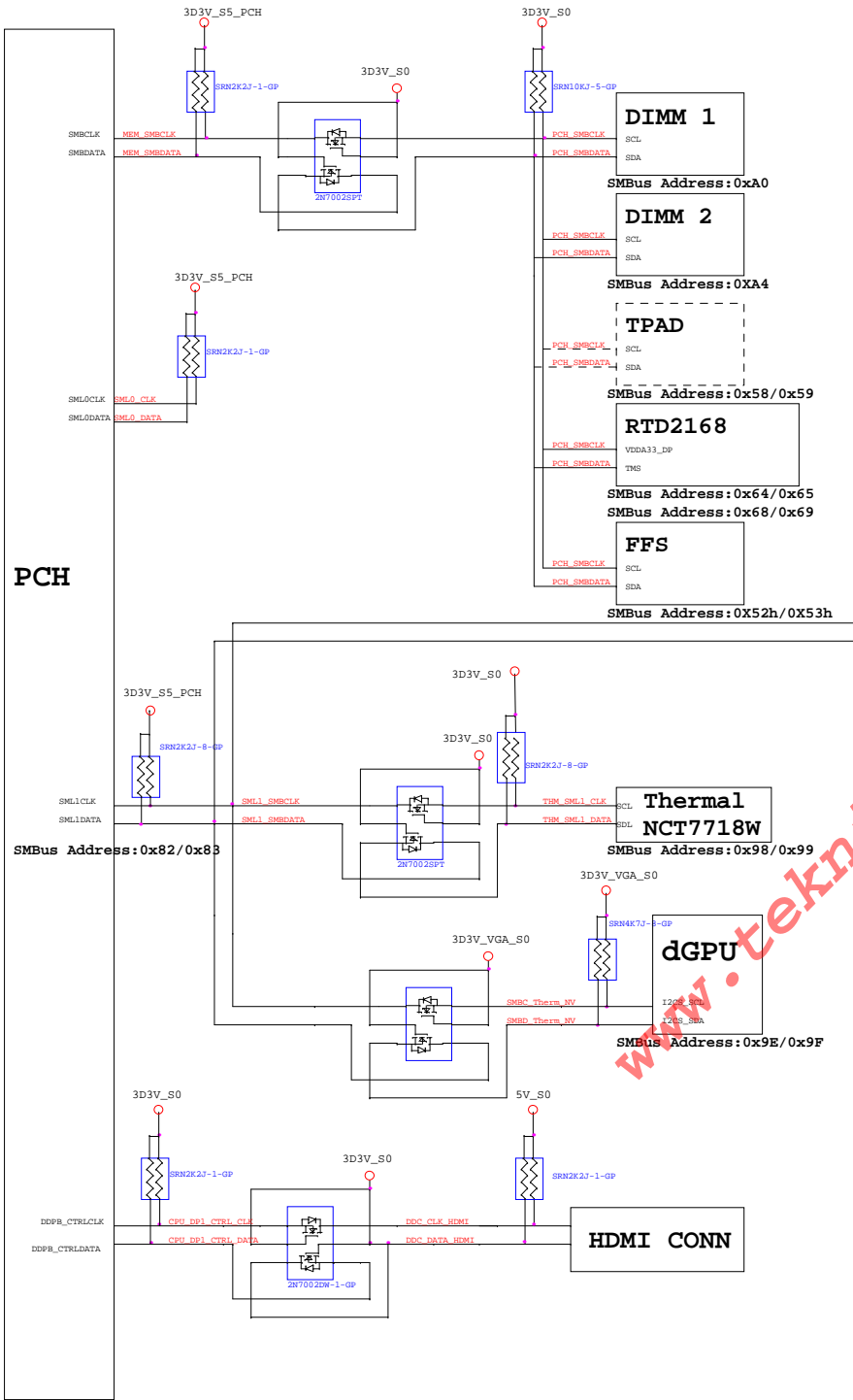




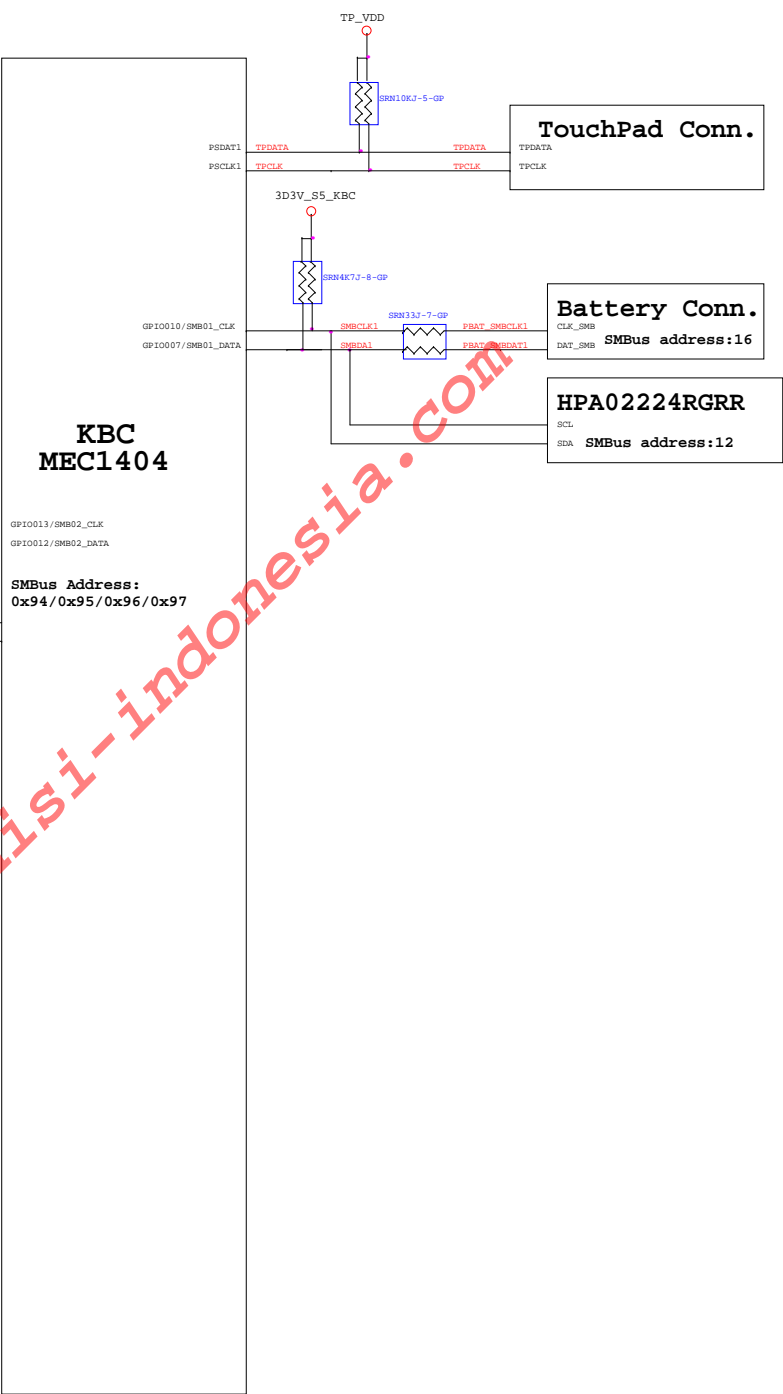
Taos Power Block Diagram



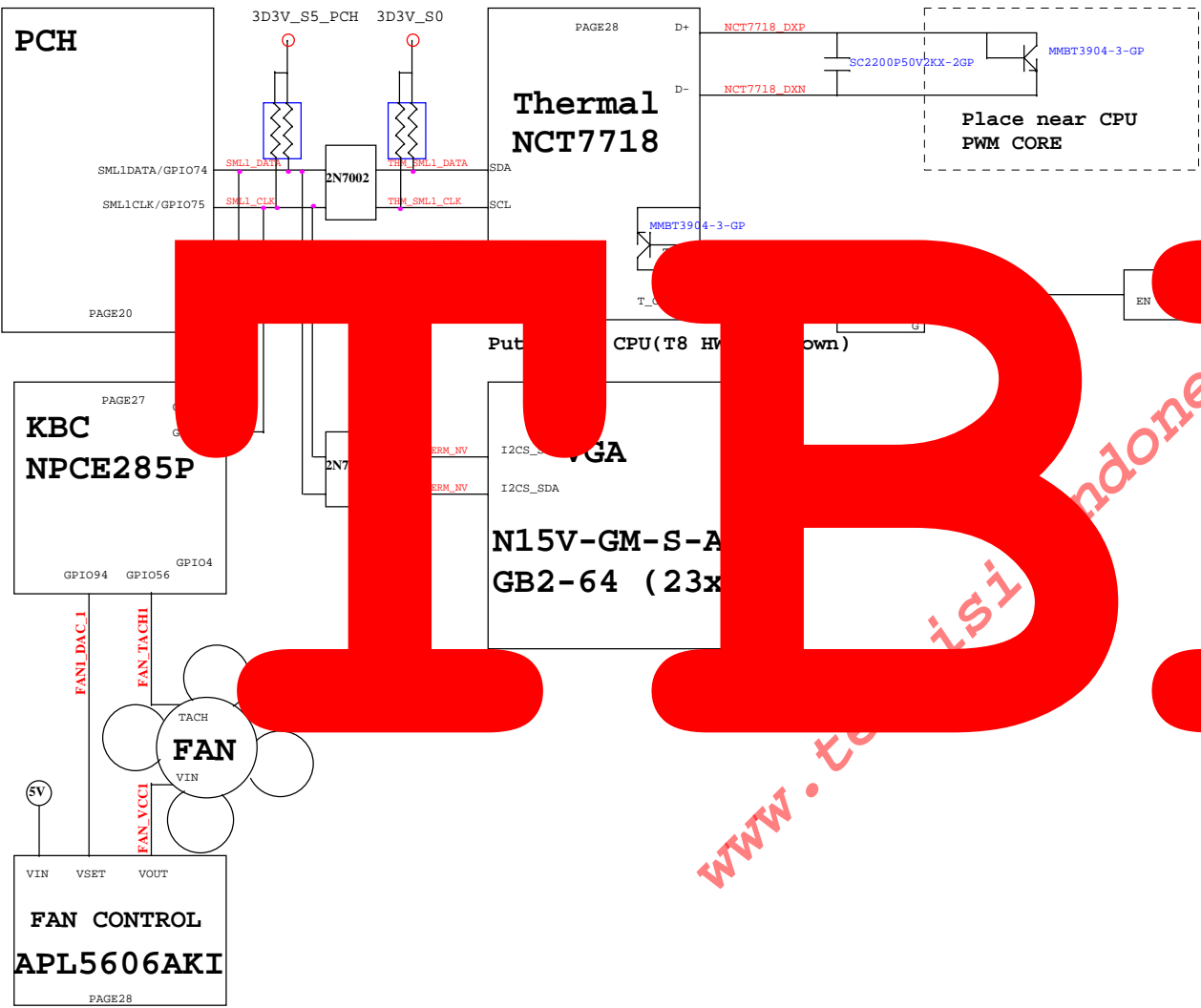
PCH SMBus Block Diagram



KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram

